

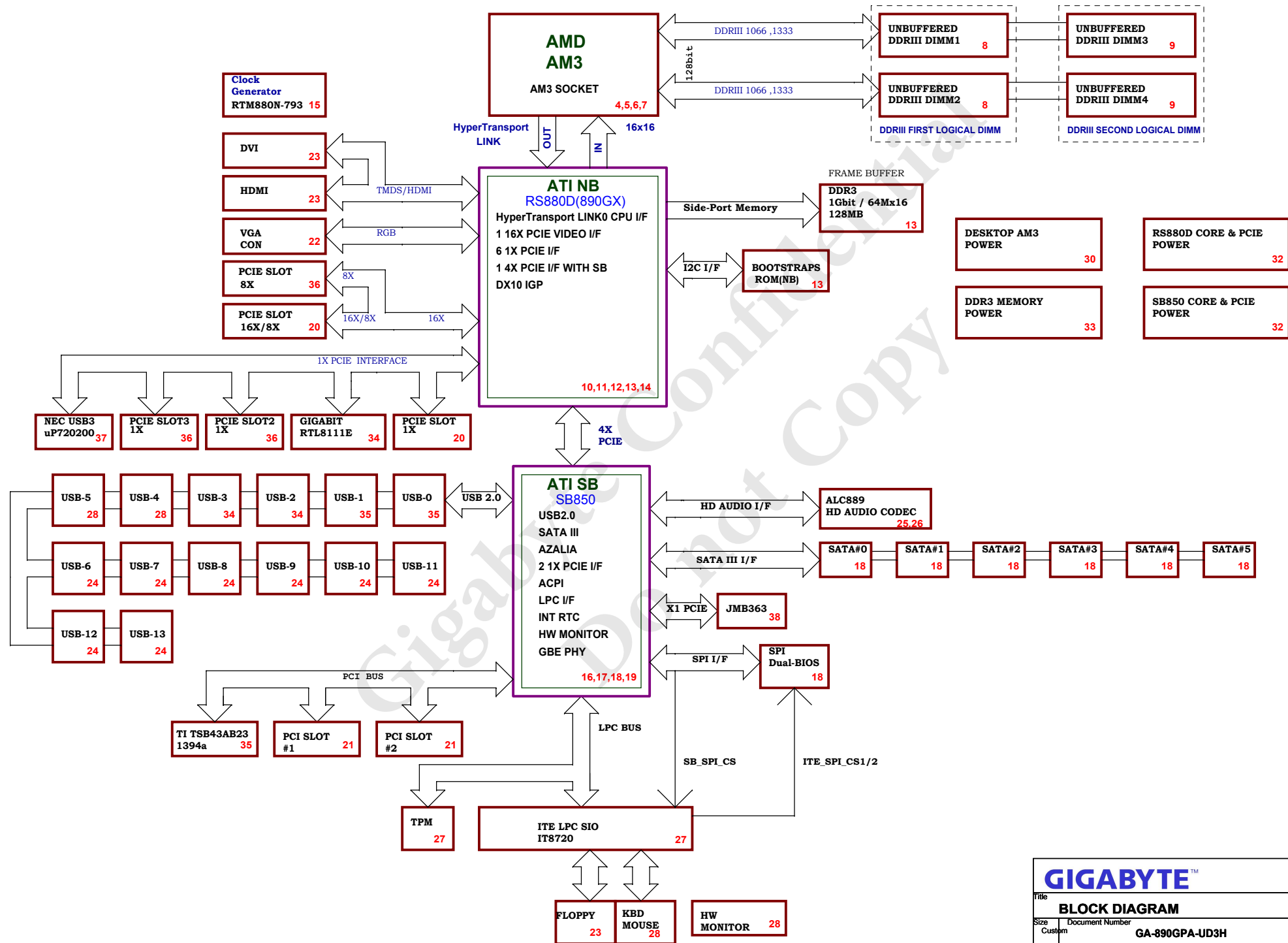
PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RS880 HT-LINK I/F
11	RS880 PCIE I/F ,SWITCH
12	RS880 SYSTEM I/F
13	RS880 STRAPS ,SPMEM
14	RS880 POWER & GND
15	RTM880N-793
16	ATI SB850 PCIE/PCI/CPU/LPC
17	ATI SB850 ACPI/USB/GPIO/AUDIO
18	ATI SB850 SATA/SPI/IDE/HWM
19	ATI SB850 POWER & GND
20	PCI EXPRESS x16 ,x1
21	PCI SLOT 1, 2
22	RGB CONNECTOR
23	FDD ,HDMI ,DVI Connector
24	COM/F_USB/I_PWR
25	ALC889

[illegible]

P-Code: U98137-0

[illegible][illegible]

RS880 CUSTOMER DESKTOP REFERENCE DESIGN

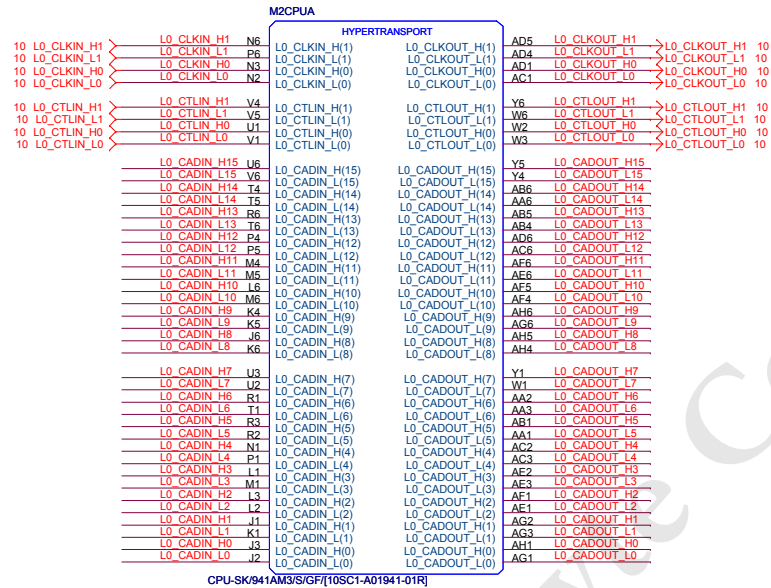


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BLOCK DIAGRAM

Title	Document Number	Rev
Size	GA-890GPA-UD3H	3.01
Custom		
Date:	Monday, January 10, 2011	Sheet 3 of 38

L0_CADIN_L[0..15] < L0_CADIN_L[0..15] 10
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 10

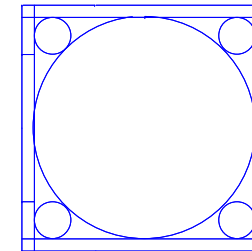


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

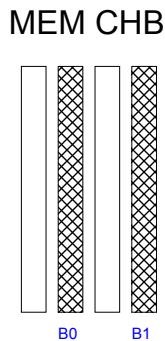
VLDT_A = VCC12_HT
 VLDT_B = HT12B

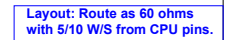
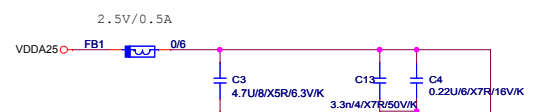
M2CPU

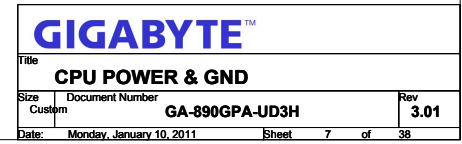
AM2RM/PP/BU/PB[12KRC-04K812-12R]

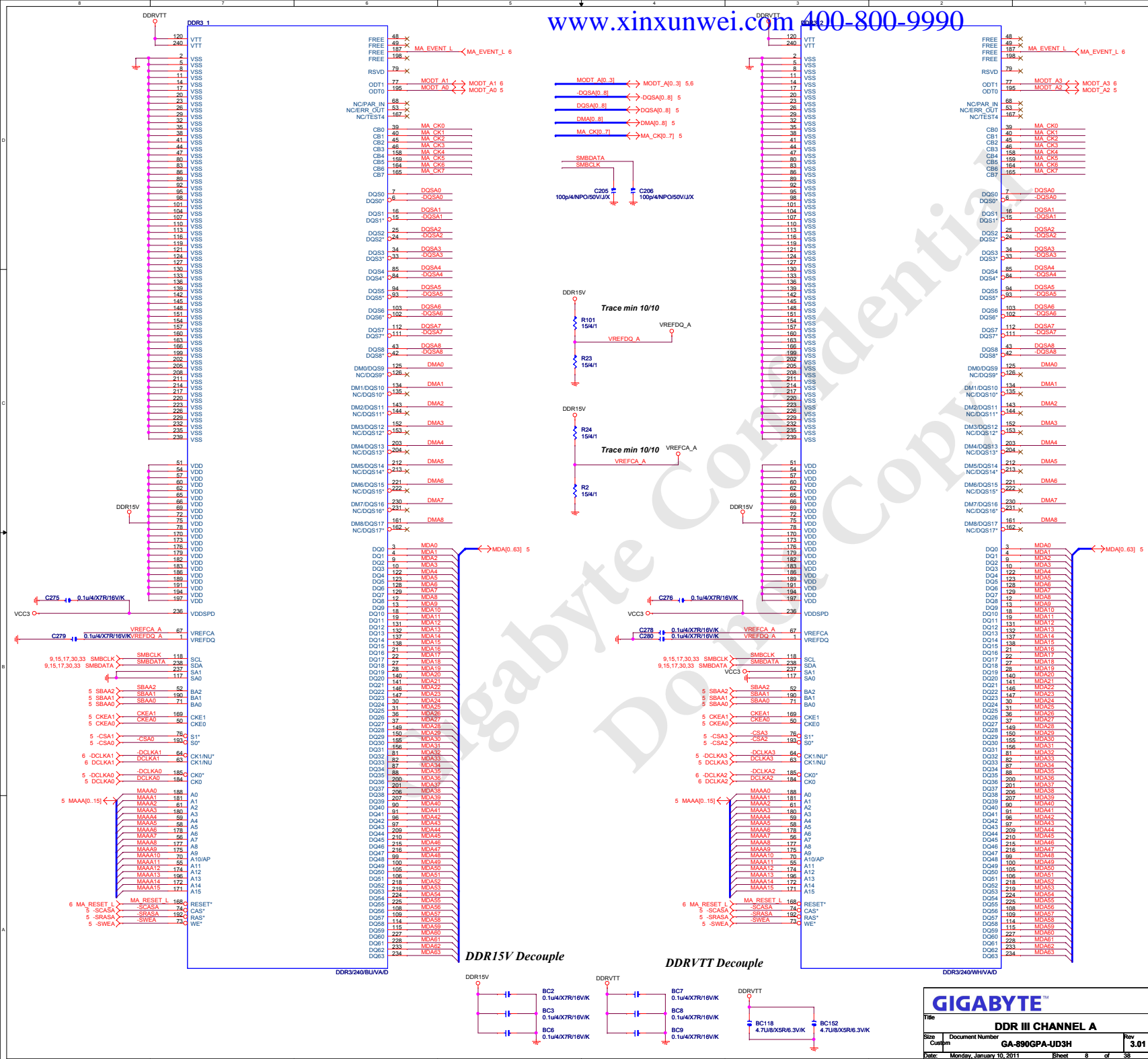

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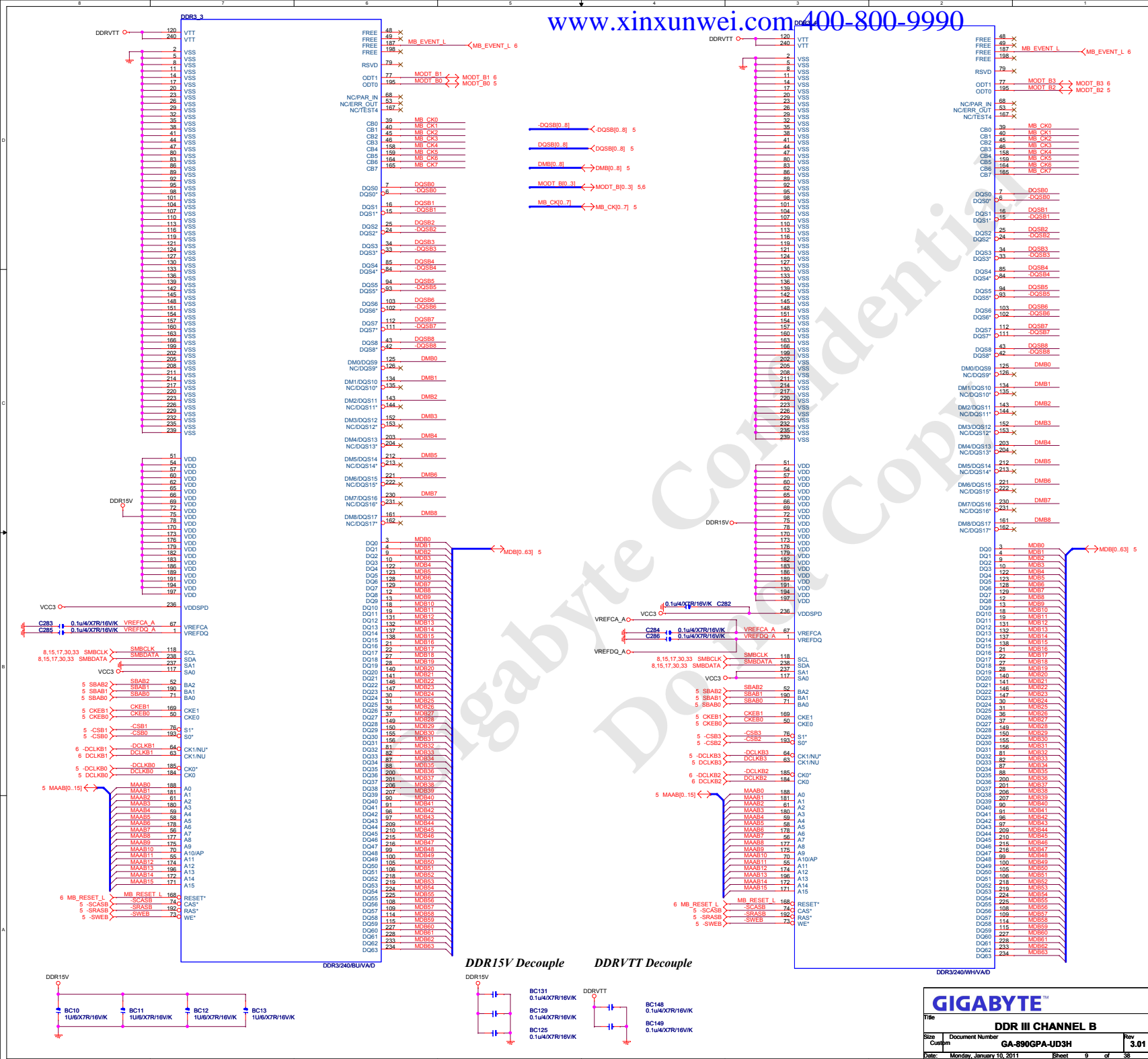
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-890GPA-UD3H	3.01	
Date:	Monday, January 10, 2011	Sheet	4 of 38

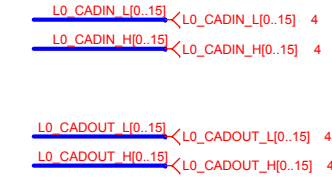
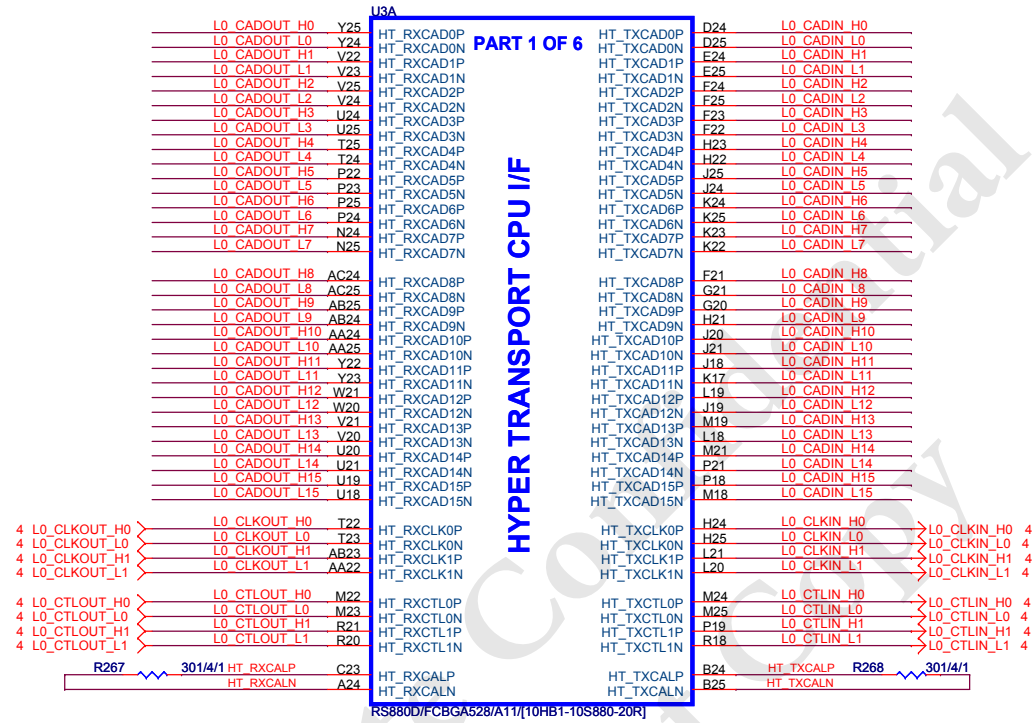




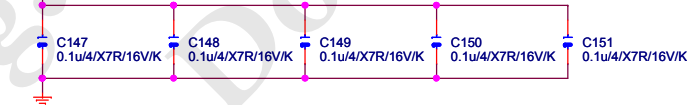




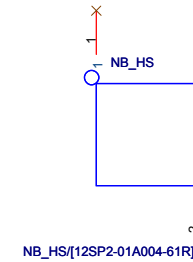




VCORE



HT Link Stitching Caps

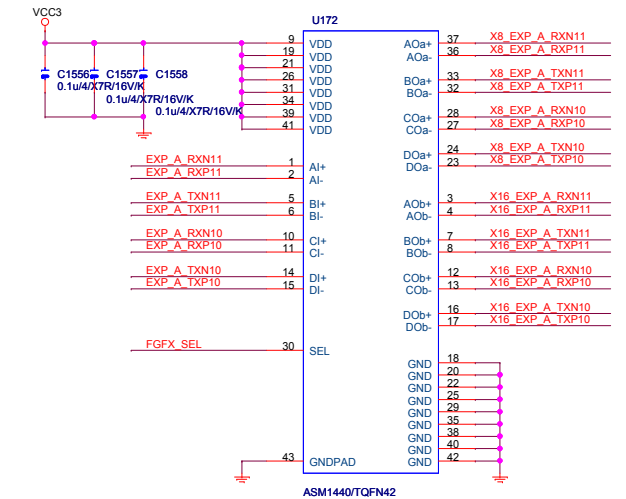
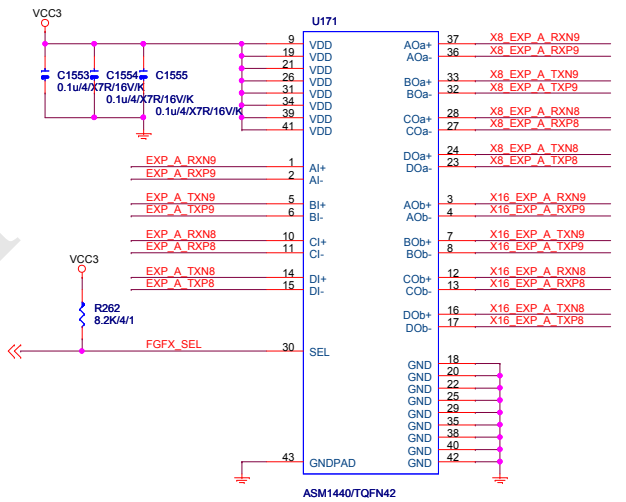
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Title		
RS880 HT-LINK I/F		
Size	Document Number	Rev
B	GA-890GPA-UD3H	3.01
Date:	Monday, January 10, 2011	Sheet 10 of 38

EXP_A_RXP[0..7] >> EXP_A_RXP[0..7] 20
EXP_A_RXN[0..7] >> EXP_A_RXN[0..7] 20

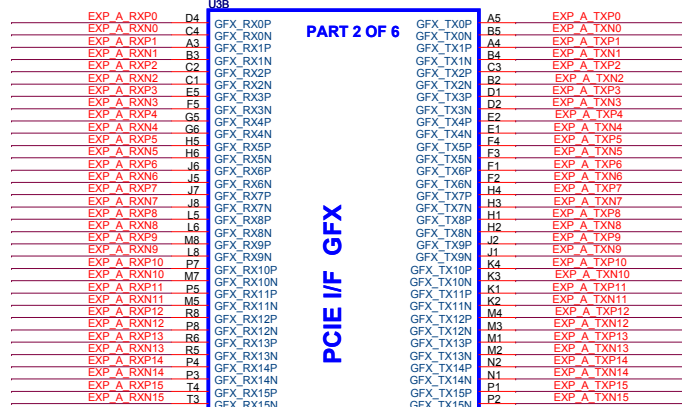
EXP_A_TXP[0..7] >> EXP_A_TXP[0..7] 20
EXP_A_TXN[0..7] >> EXP_A_TXN[0..7] 20

Function	SEL
$xI \rightarrow xOa$	L (X8)
$xI \rightarrow xOb$	H (X16)

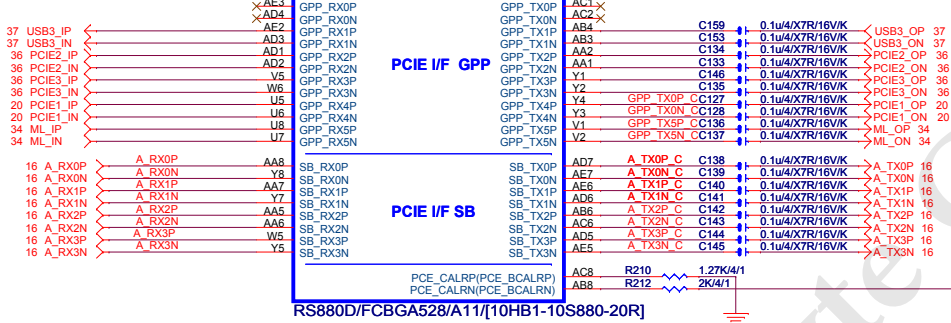


PART 2 OF 6

PCIE I/F GFX

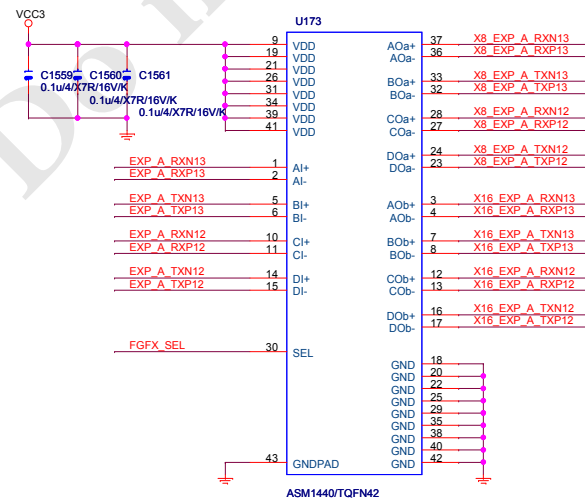
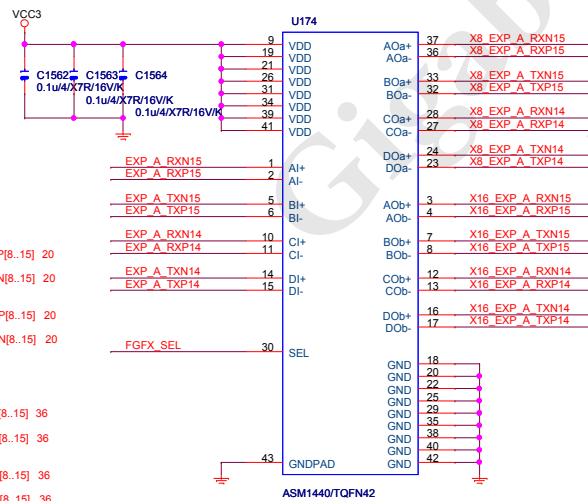


PCIE I/F GPP



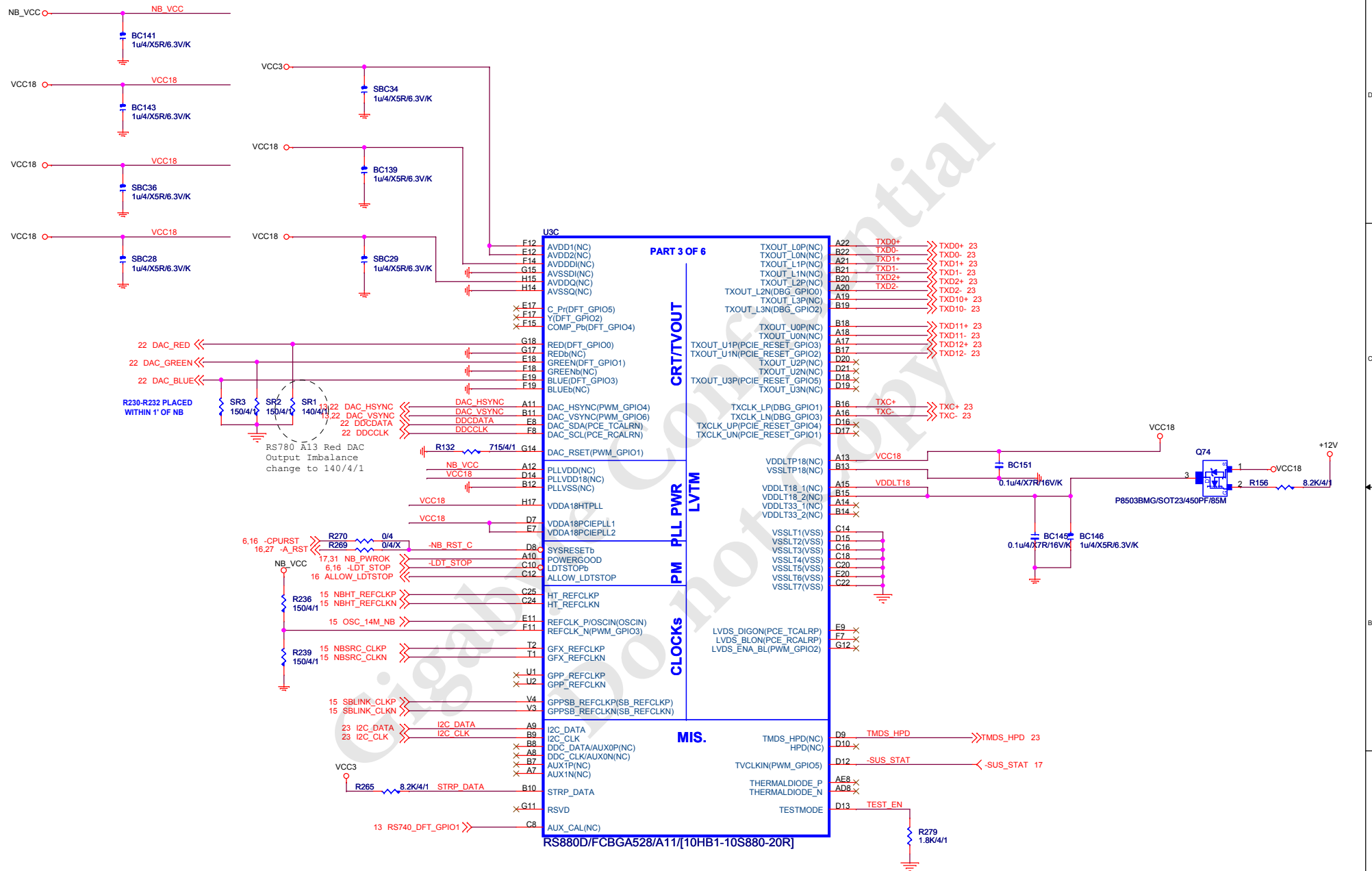
PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

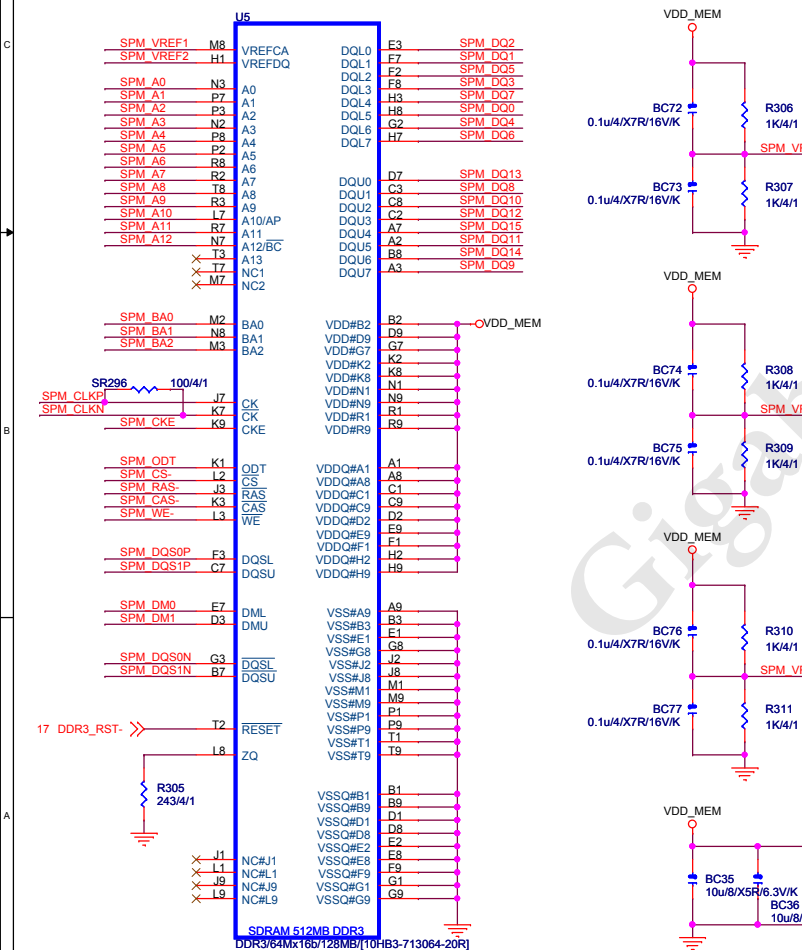
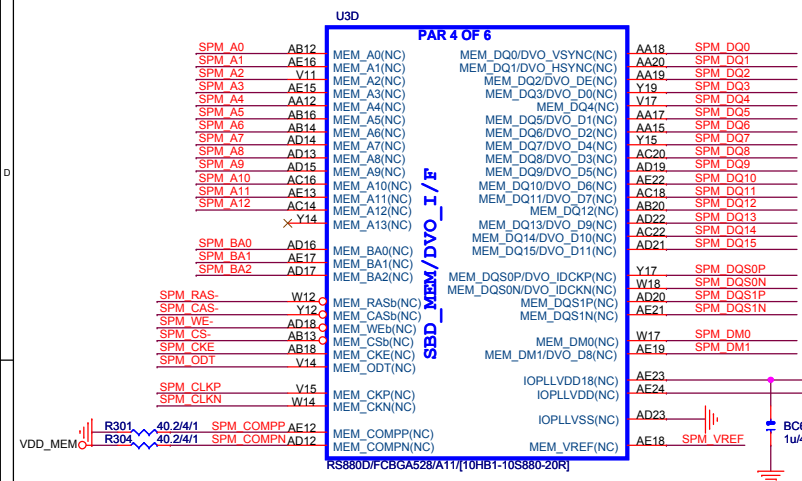
RS880D/FCBGA528/A11/[10HB1-10S880-20R]



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Title	RS880 PCIE I/F Switch	
Size	Document Number	Rev
Custom	GA-890GPA-UD3H	3.01
Date:	Monday, January 10, 2011	Sheet 11 of 38





RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL,
place close to pin C8



Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K according!



Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780 DFT GPIO5)

```
Selects Loading of STRAPS from EPROM
```

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
RS740: pin DFT GPIO1
RS780: pin DFT GPIO1
RS780: pin SUS STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)      default
110: 4-0-0-0-0-0    Config A
101: 4-4-0-0-0-0    Config B
100: 4-2-2-0-0-0    Config C
011: 4-2-1-1-0-0    Config D
010: 4-1-1-1-1-1    Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

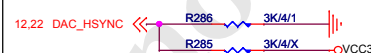
```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0]
(configure thru register setting)

1-1-1-1-1-1	Mode L	default
1-1-1-1-1-1	Mode L	
2-0-2-0-2-0	Mode C2	
2-0-2-0-1-1	Mode K	
2-0-1-1-1-1	Mode E	
1-1-1-1-1-1	Mode L	
4-0-0-0-1-1	Mode C	
4-0-0-0-2-0	Mode B	

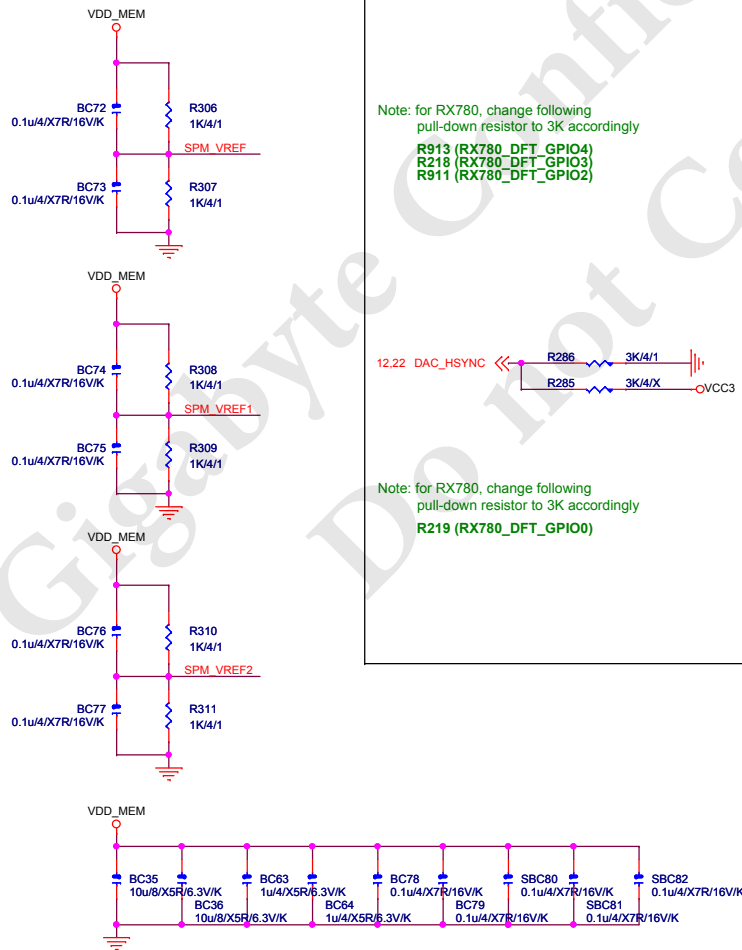
RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Applicable
```

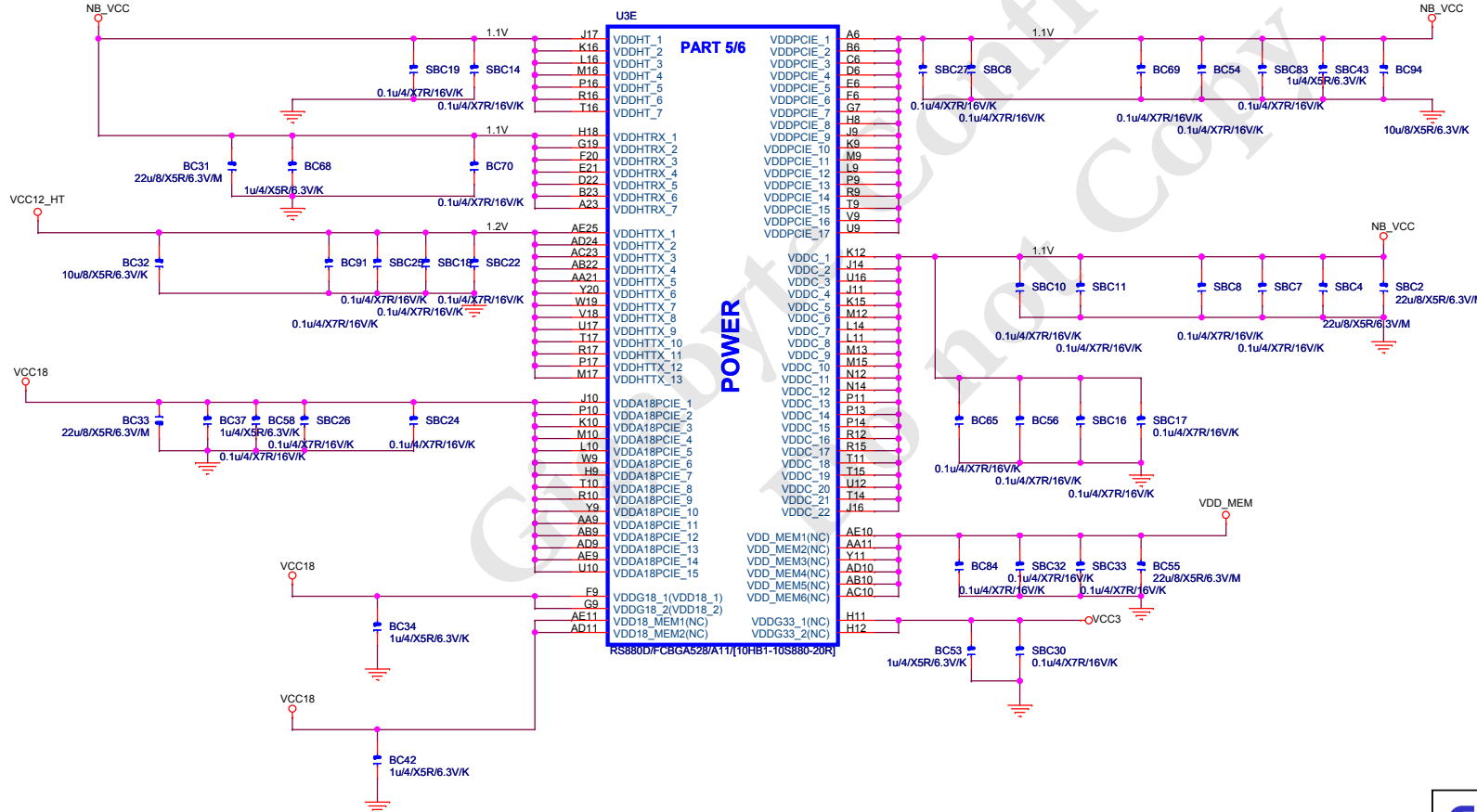
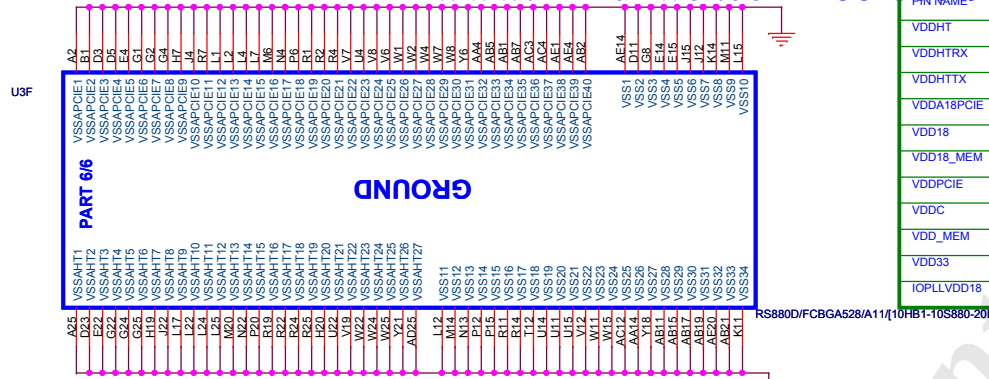


RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
   thru nbpcf register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
      setting only
RS740: Not supported
```



RS880 POWER DIFFERENCE TABLE				RS880 POWER DIFFERENCE TABLE			
PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



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Title
RS880 POWER & GNDSize
Custom Document Number
GA-890GPA-UD3HRev
3.01

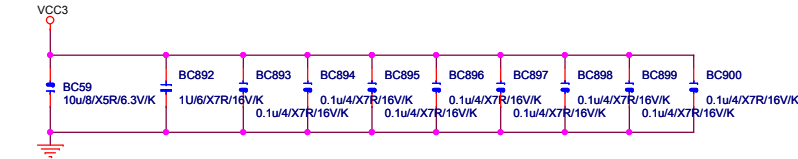
Date: Monday, January 10, 2011

Sheet 14 of 38

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

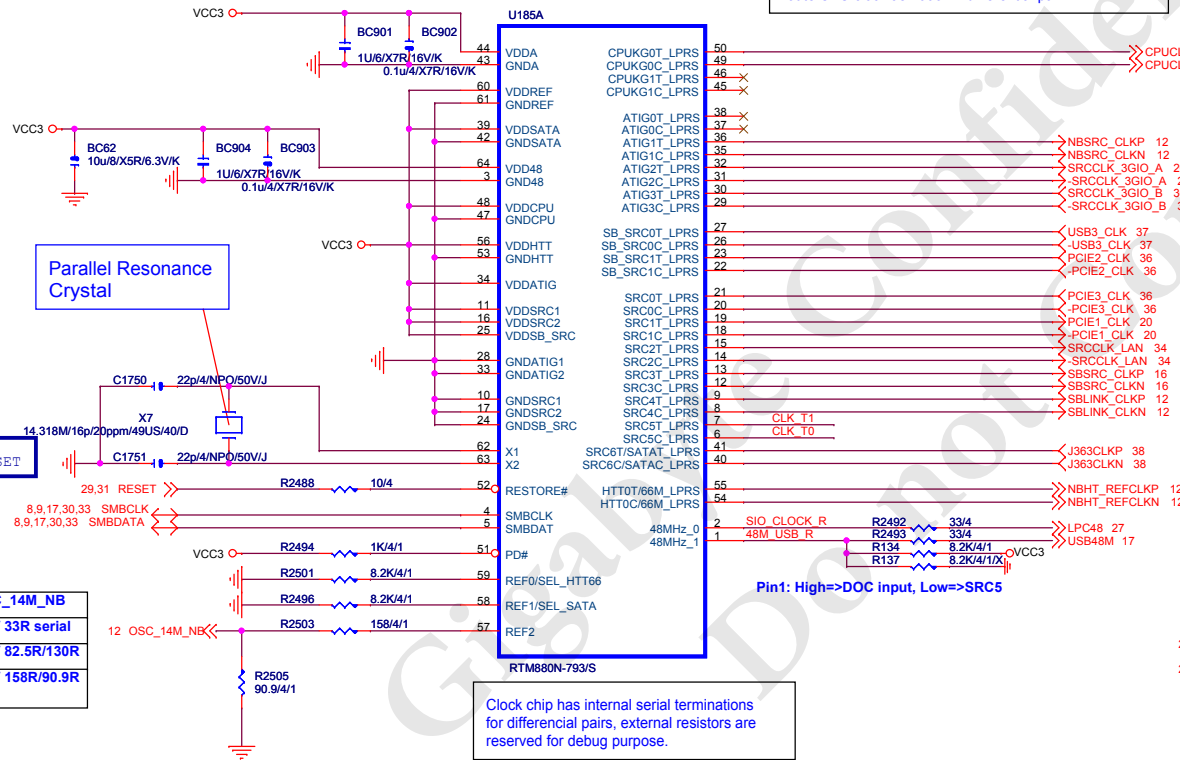
* the GFX_REFCLK input is required for all cases



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

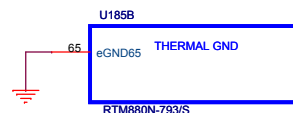


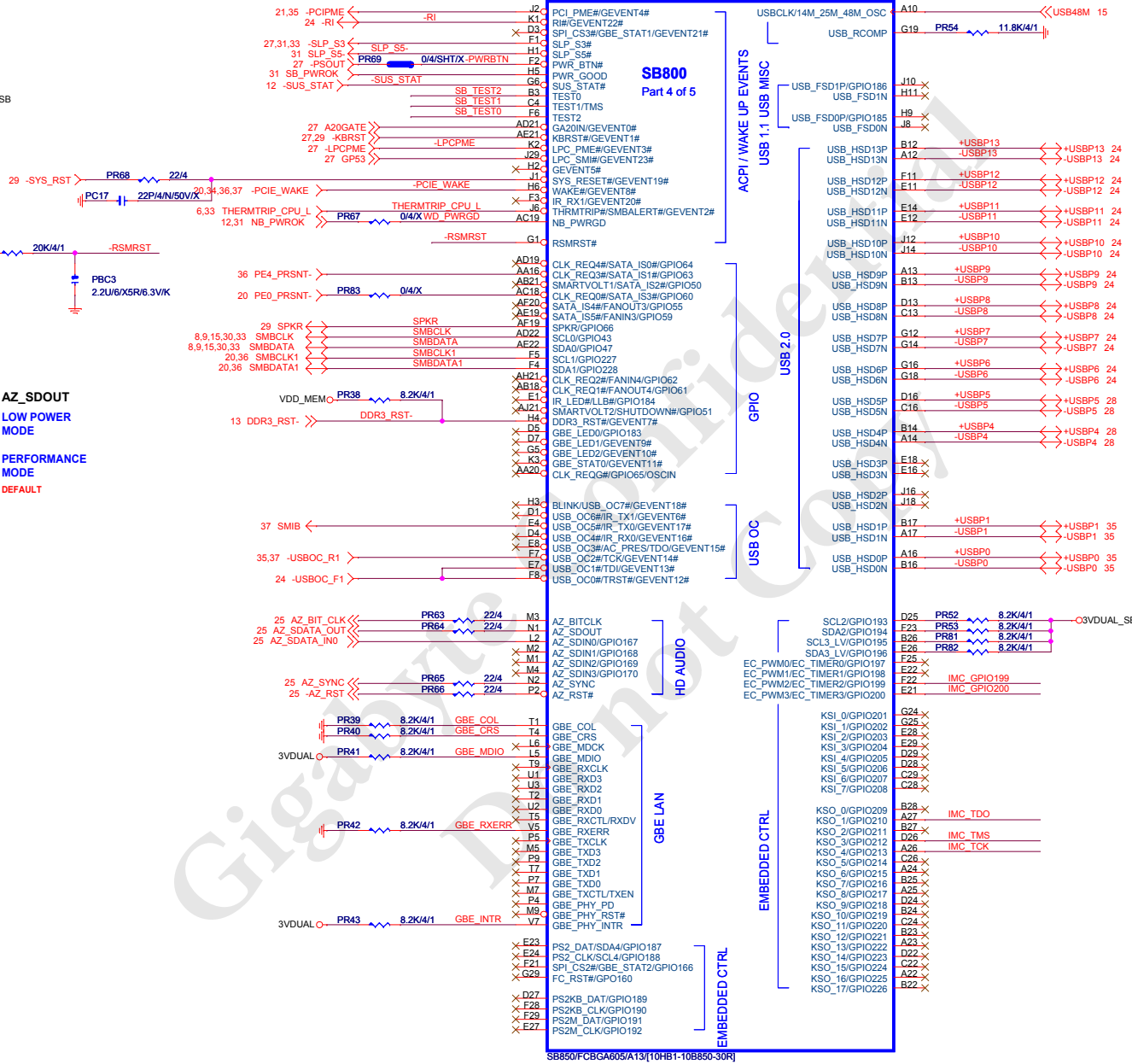
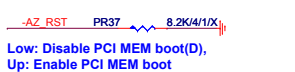
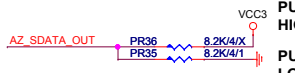
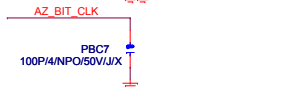
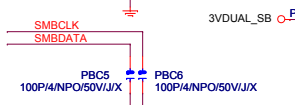
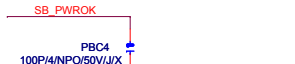
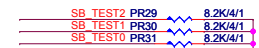
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

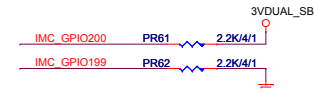
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.





USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals
can be used for power-up sequencer



IMC_GPIO200 IMC_GPIO199

ROM TYPE:

II. II – Background

H, H = Reserved

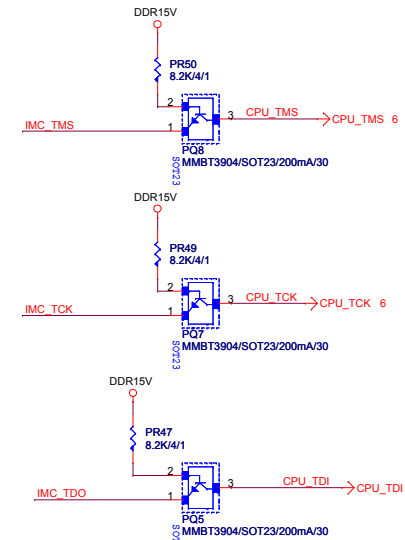
H. L = SPI ROM

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L, H = LPC ROM

 $\Delta I = \text{FWHM ROI}$

E, E = 1 WITH RO

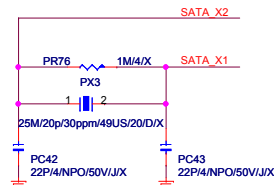
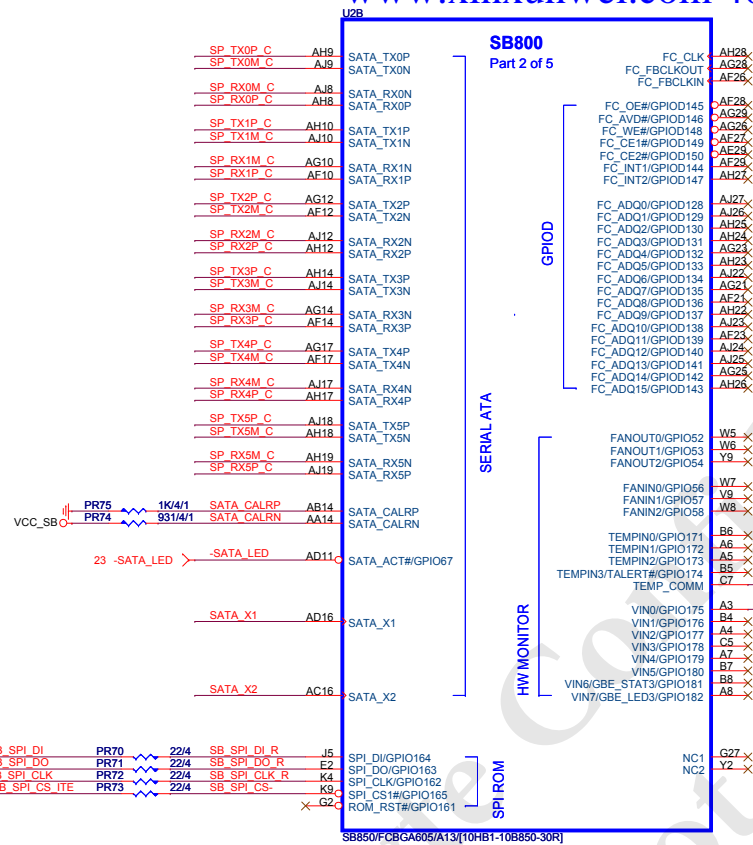


GIGABYTE

Title
ATI SB850 ACPI/USB/GPIO/AUDIO

| | | |
|--------|-----------------|------|
| Size | Document Number | Rev |
| Custom | GA-890GPA-J1D3H | 3.01 |

Date: Monday, January 10, 2011 Sheet 17 of 38



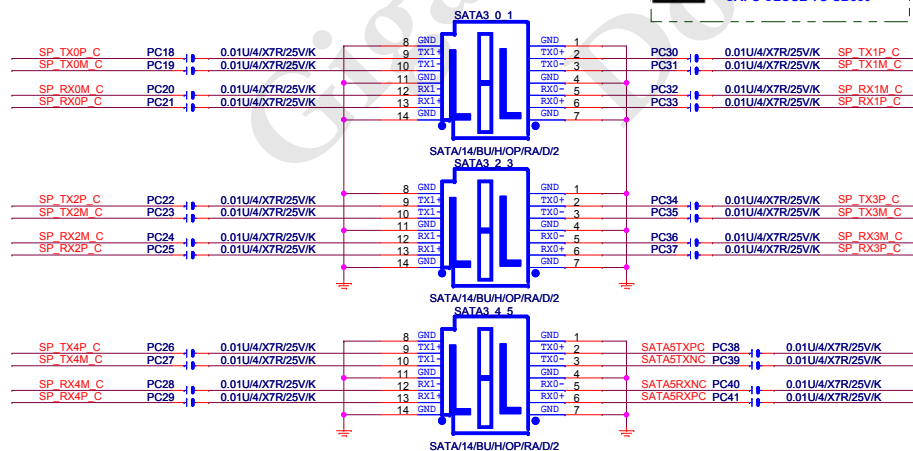
PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE :

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

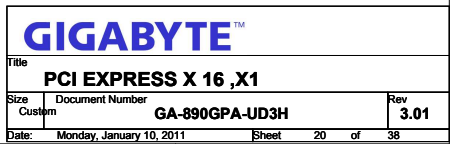


| U2E | | SB800 | |
|------|------------------|------------------|------|
| Y14 | VSSIO_SATA_1 | VSS_1 | A12 |
| Y16 | VSSIO_SATA_2 | VSS_2 | A28 |
| AB16 | VSSIO_SATA_3 | VSS_3 | A2 |
| AC14 | VSSIO_SATA_4 | VSS_4 | E5 |
| AE12 | VSSIO_SATA_5 | VSS_5 | D23 |
| AE14 | VSSIO_SATA_6 | VSS_6 | E26 |
| AF11 | VSSIO_SATA_7 | VSS_7 | E6 |
| AF13 | VSSIO_SATA_8 | VSS_8 | F24 |
| AF16 | VSSIO_SATA_9 | VSS_9 | N15 |
| AG8 | VSSIO_SATA_10 | VSS_10 | R13 |
| AH7 | VSSIO_SATA_11 | VSS_11 | R17 |
| AH11 | VSSIO_SATA_12 | VSS_12 | T10 |
| AH13 | VSSIO_SATA_13 | VSS_13 | P10 |
| AH16 | VSSIO_SATA_14 | VSS_14 | V11 |
| AJ7 | VSSIO_SATA_15 | VSS_15 | U15 |
| AJ11 | VSSIO_SATA_16 | VSS_16 | M18 |
| AJ13 | VSSIO_SATA_17 | VSS_17 | V19 |
| AJ16 | VSSIO_SATA_18 | VSS_18 | M11 |
| | VSSIO_SATA_19 | VSS_19 | L12 |
| | | VSS_20 | L18 |
| A9 | VSSIO_USB_1 | VSS_21 | P3 |
| B10 | VSSIO_USB_2 | VSS_22 | P3 |
| K11 | VSSIO_USB_3 | VSS_23 | V4 |
| B9 | VSSIO_USB_4 | VSS_24 | A06 |
| D10 | VSSIO_USB_5 | VSS_25 | A04 |
| D12 | VSSIO_USB_6 | VSS_26 | A87 |
| D14 | VSSIO_USB_7 | VSS_27 | AC9 |
| D17 | VSSIO_USB_8 | VSS_28 | V8 |
| E9 | VSSIO_USB_9 | VSS_29 | W9 |
| F9 | VSSIO_USB_10 | VSS_30 | W10 |
| F12 | VSSIO_USB_11 | VSS_31 | A28 |
| F14 | VSSIO_USB_12 | VSS_32 | B29 |
| F16 | VSSIO_USB_13 | VSS_33 | U4 |
| G9 | VSSIO_USB_14 | VSS_34 | Y18 |
| G11 | VSSIO_USB_15 | VSS_35 | Y12 |
| H9 | VSSIO_USB_16 | VSS_36 | Y11 |
| H12 | VSSIO_USB_17 | VSS_37 | AA11 |
| H14 | VSSIO_USB_18 | VSS_38 | AA12 |
| H16 | VSSIO_USB_19 | VSS_39 | G4 |
| H18 | VSSIO_USB_20 | VSS_40 | J4 |
| J11 | VSSIO_USB_21 | VSS_41 | G8 |
| J13 | VSSIO_USB_22 | VSS_42 | G9 |
| J19 | VSSIO_USB_23 | VSS_43 | M12 |
| K12 | VSSIO_USB_24 | VSS_44 | AF29 |
| K14 | VSSIO_USB_25 | VSS_45 | H7 |
| K16 | VSSIO_USB_26 | VSS_46 | AH29 |
| K18 | VSSIO_USB_27 | VSS_47 | V10 |
| H19 | VSSIO_USB_28 | VSS_48 | P6 |
| | | VSS_49 | N4 |
| | | VSS_50 | L4 |
| Y4 | EFUSE | VSS_51 | L8 |
| | | VSS_52 | |
| D8 | VSSAN_HWM | | |
| M19 | VSSXL | VSSPL_SYS | M29 |
| P21 | VSSIO_PCIECLK_1 | VSSIO_PCIECLK_14 | H23 |
| P22 | VSSIO_PCIECLK_2 | VSSIO_PCIECLK_15 | H26 |
| M20 | VSSIO_PCIECLK_3 | VSSIO_PCIECLK_16 | AA21 |
| M24 | VSSIO_PCIECLK_4 | VSSIO_PCIECLK_17 | AA23 |
| M26 | VSSIO_PCIECLK_5 | VSSIO_PCIECLK_18 | AB23 |
| P22 | VSSIO_PCIECLK_6 | VSSIO_PCIECLK_19 | AD23 |
| P24 | VSSIO_PCIECLK_7 | VSSIO_PCIECLK_20 | AC26 |
| P26 | VSSIO_PCIECLK_8 | VSSIO_PCIECLK_21 | Y20 |
| T20 | VSSIO_PCIECLK_9 | VSSIO_PCIECLK_22 | W21 |
| T22 | VSSIO_PCIECLK_10 | VSSIO_PCIECLK_23 | W20 |
| T24 | VSSIO_PCIECLK_11 | VSSIO_PCIECLK_24 | AE26 |
| V20 | VSSIO_PCIECLK_12 | VSSIO_PCIECLK_25 | L24 |
| J23 | VSSIO_PCIECLK_13 | VSSIO_PCIECLK_26 | K20 |
| | | VSSIO_PCIECLK_27 | |

Part 5 of 5

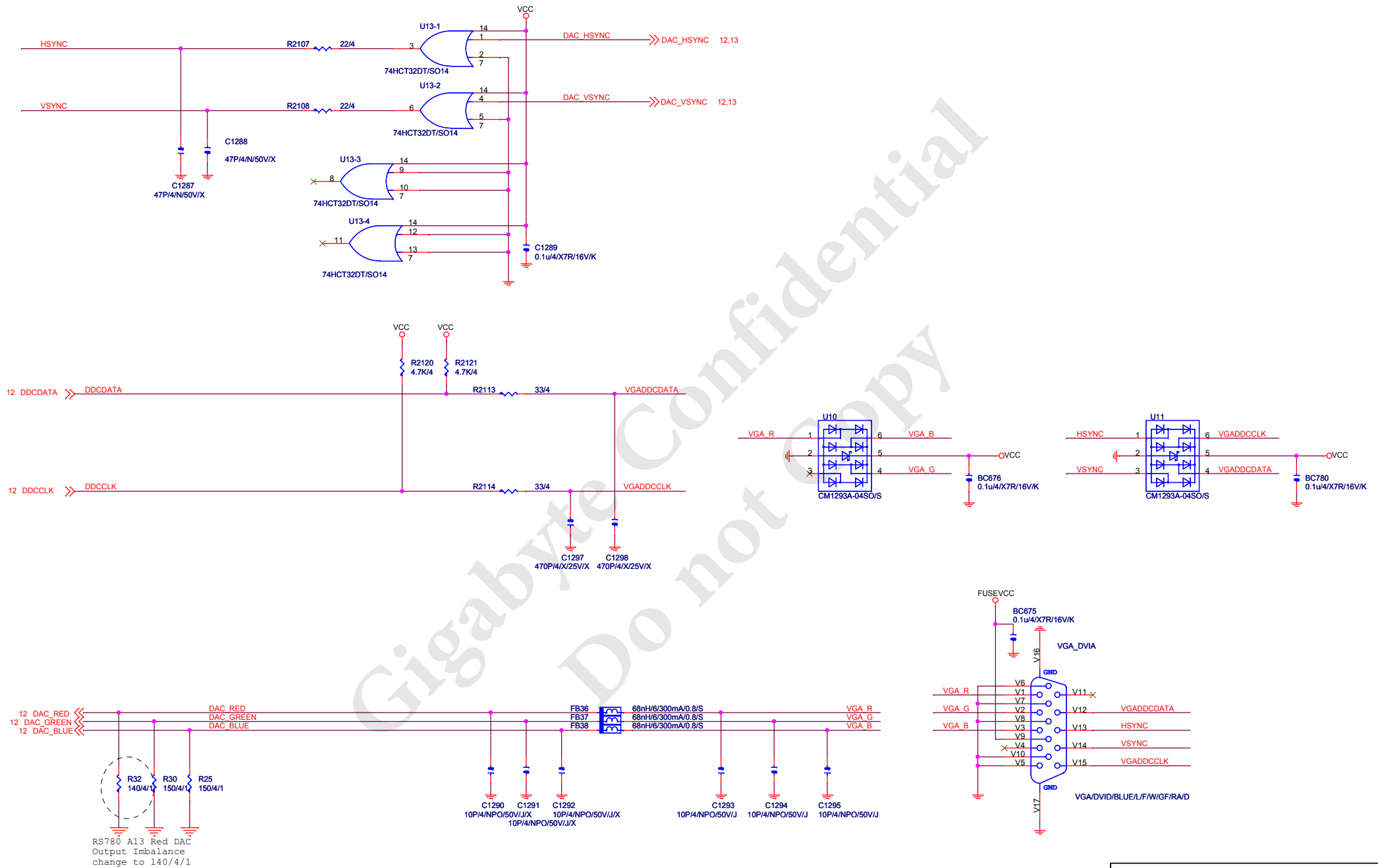
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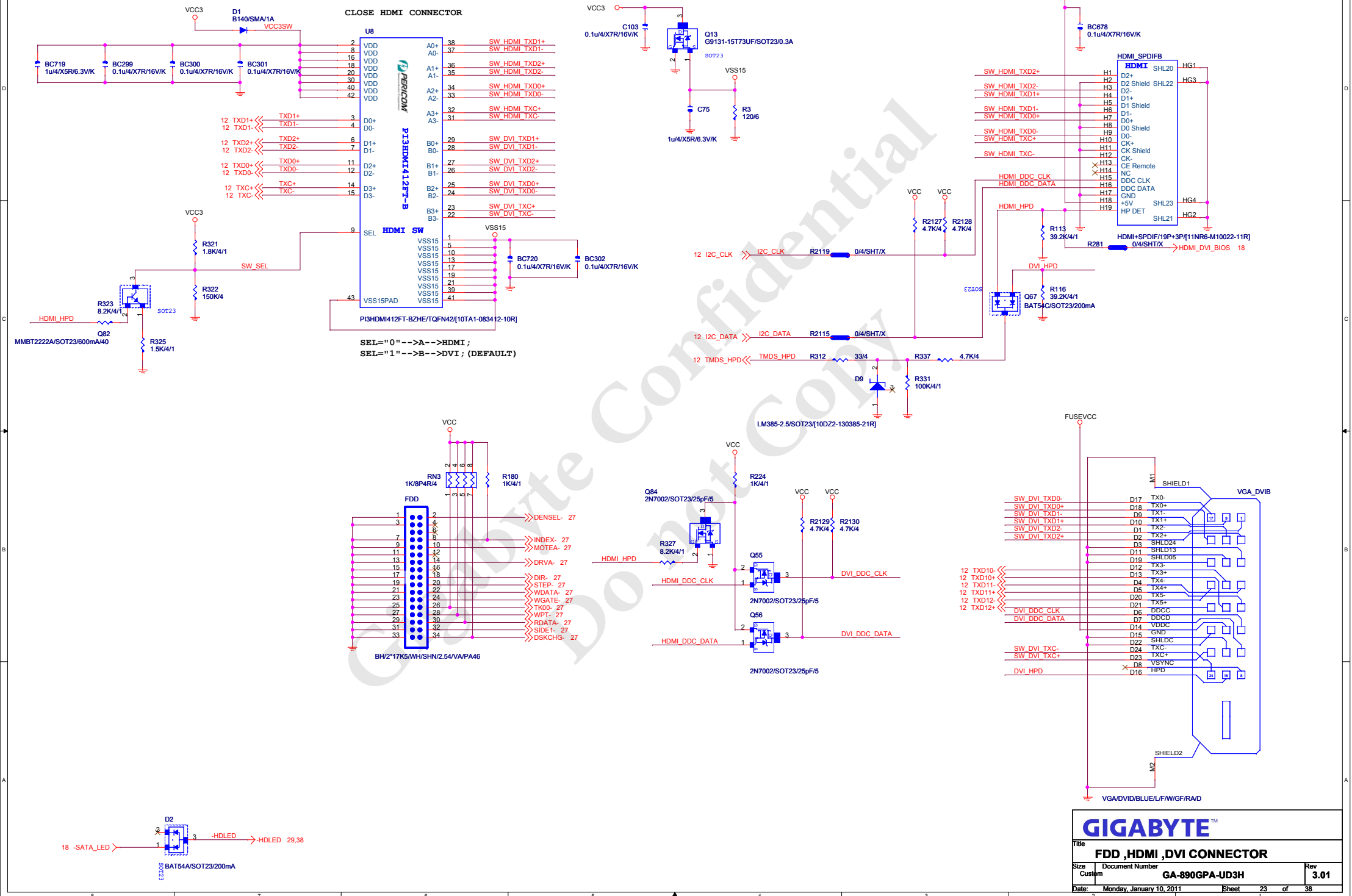
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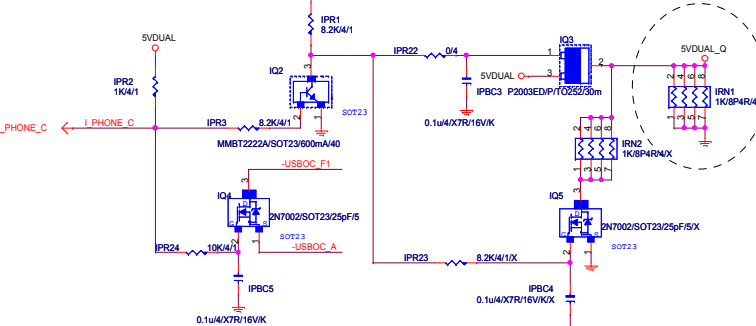
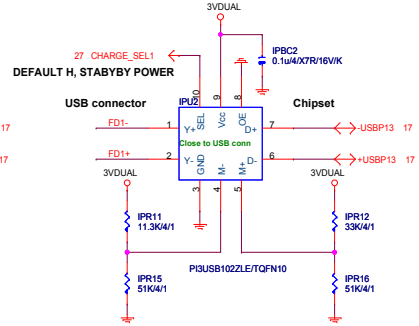
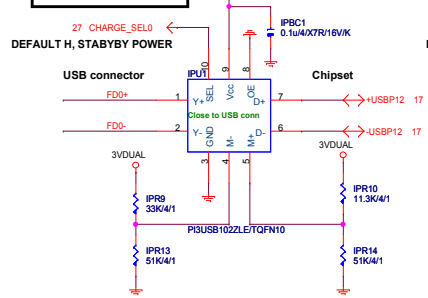
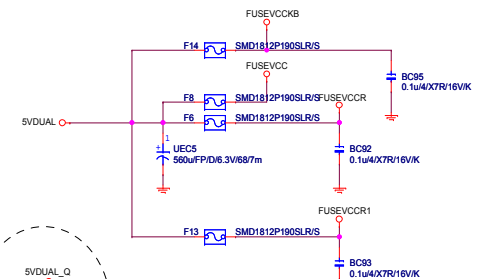
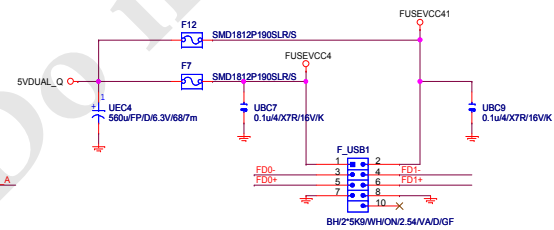
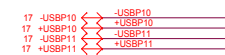
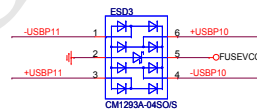
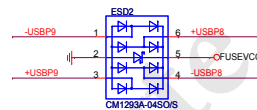
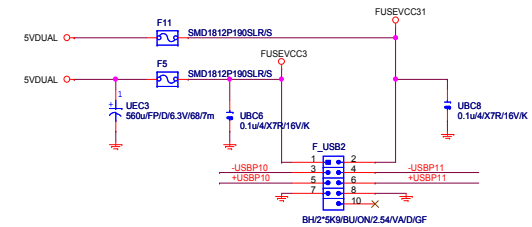
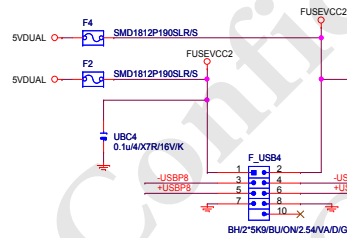
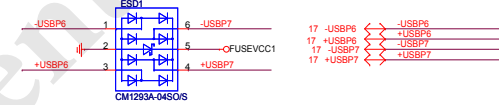
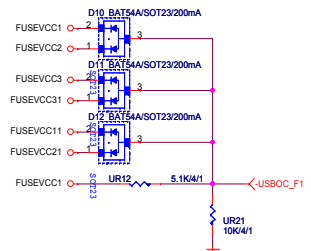
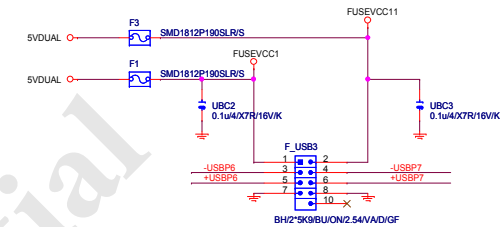
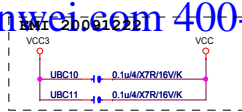
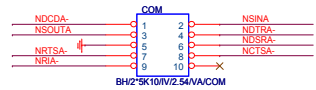




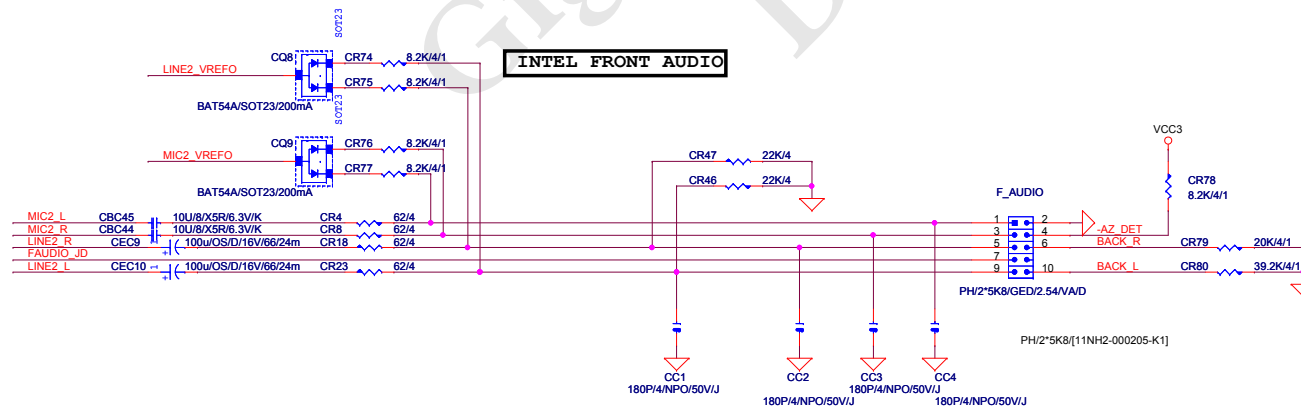
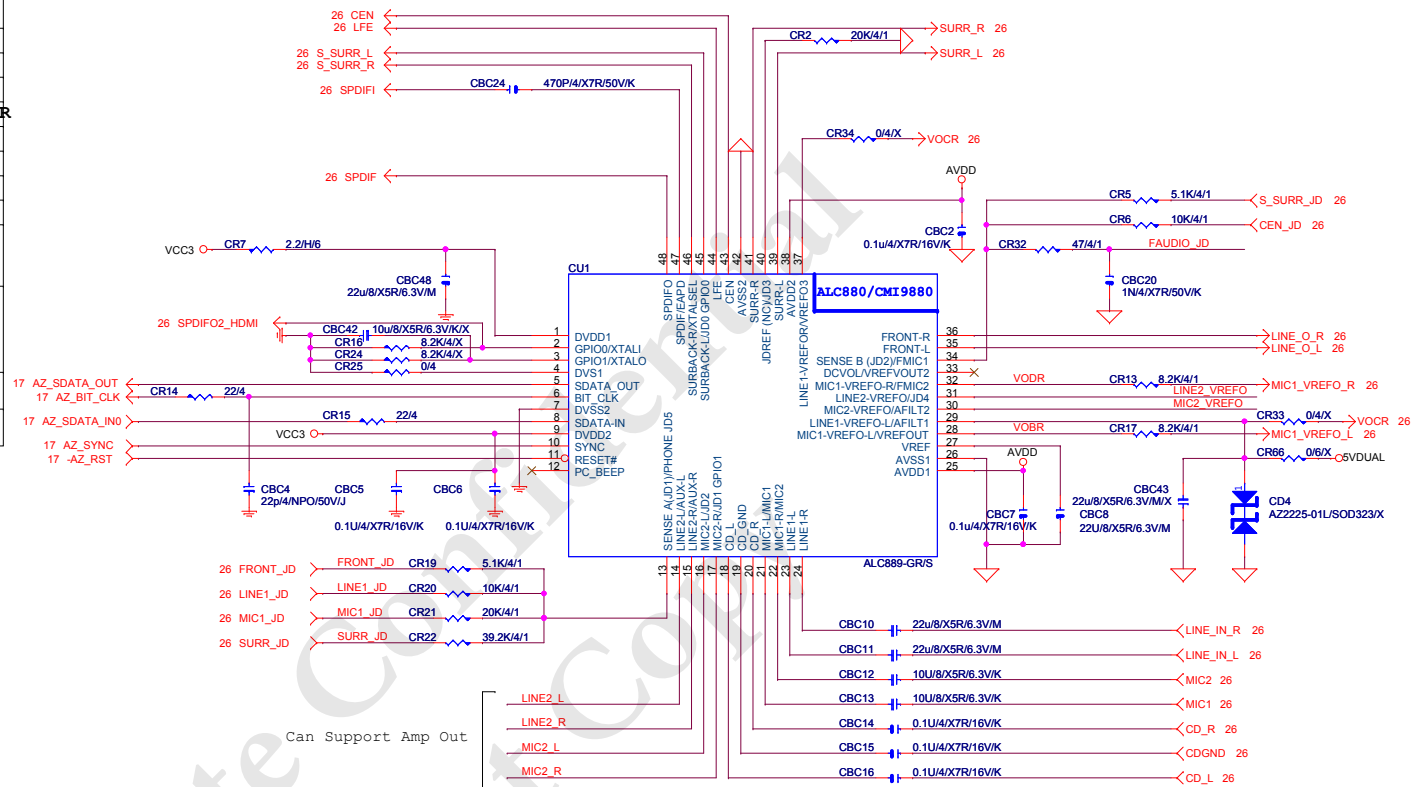
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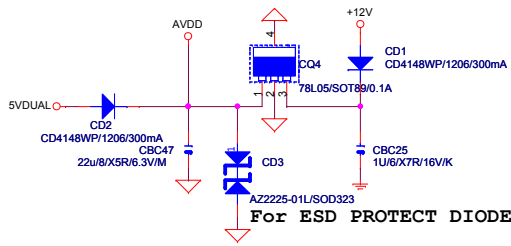
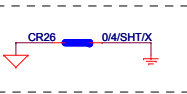




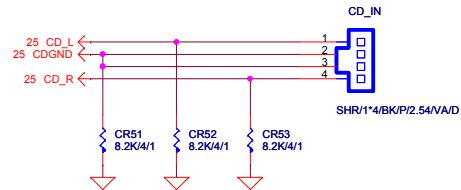


| | ALC892R | ALC889 | ALC889A | ALC888 | ALC892 |
|-------------------------------------------------------------------------------------------|---------------|-----------------------|---------------|---------------|---------------|
| CR16 | X | X | O | X | X |
| CR24 | X | X | O | X | X |
| CR25 | X | O | O | O | X |
| CBC42 | 10uF/X5R | X | X | X | 10uF/X5R |
| CR2 | 20K/1% | 20K/1% | 20K/0.1% | 20K/1% | 20K/1% |
| CR9 | O | O | X | X | O |
| CR10 | X | X | O | O | X |
| CBC10/CBC11/CBC12/
CBC13/CBC44/CBC45 | 4.7uF
/X5R | 10uF
/X5R | 4.7uF
/X5R | 4.7uF
/X5R | 4.7uF
/X5R |
| CR4/CR8/CR18/CR23/
CR11/CR12/CR27/CR29/
CR49/CR50/CR43/CR44/
CR45/CR48/CR59/CR60 | 75 ohm | 66 ohm
or
lower | 75 ohm | 75 ohm | 75 ohm |
| CR33/CD1/CD2/CD3/CQ4/
CBC25 | O | O | O | O | X |
| CR34/CR66/CBC43/CD4 | X | X | X | X | O |

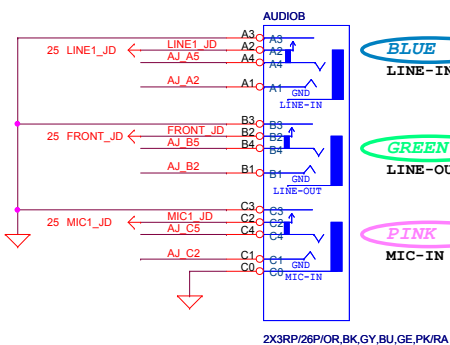
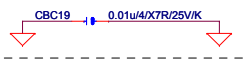




CD IN

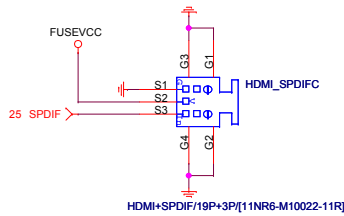
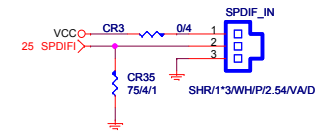
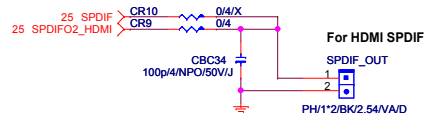


For Audio precision test

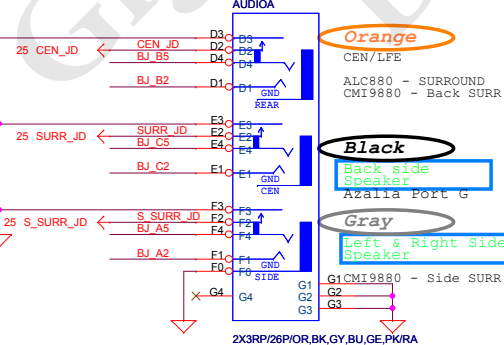
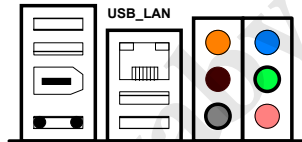


A3R3/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R3+15P/[11NR6-403004-11]

SPDIF



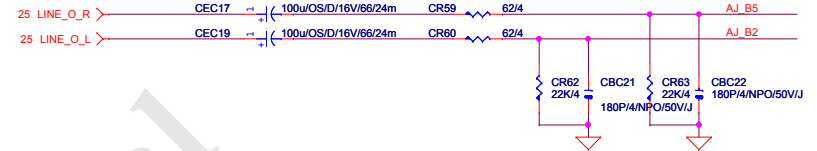
USB_1394_ESATA



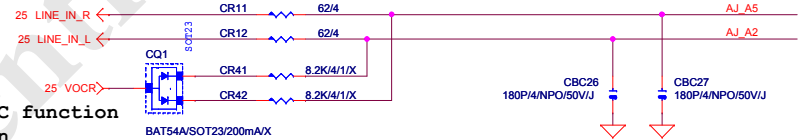
A3R3/13P/0BG/[11NR6-403006-71]
3R3+15P/[11NR6-403004-31]

www.xinxunwei.com 400-800-9990

LINE OUT FRONT OUT

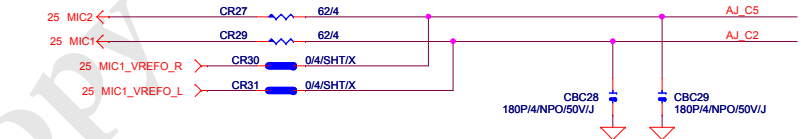


LINE-IN

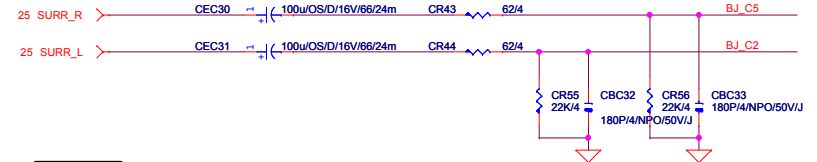


Verify MIC function
in LINE-in

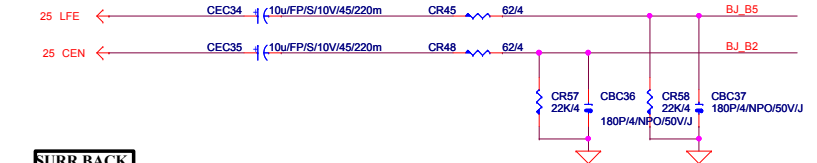
MIC



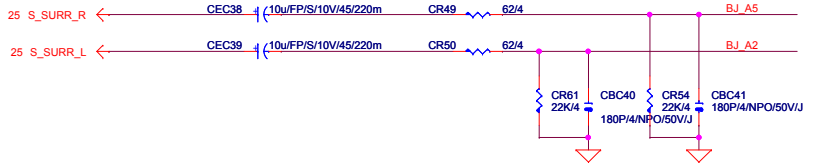
SURROUND



CEN/LFE

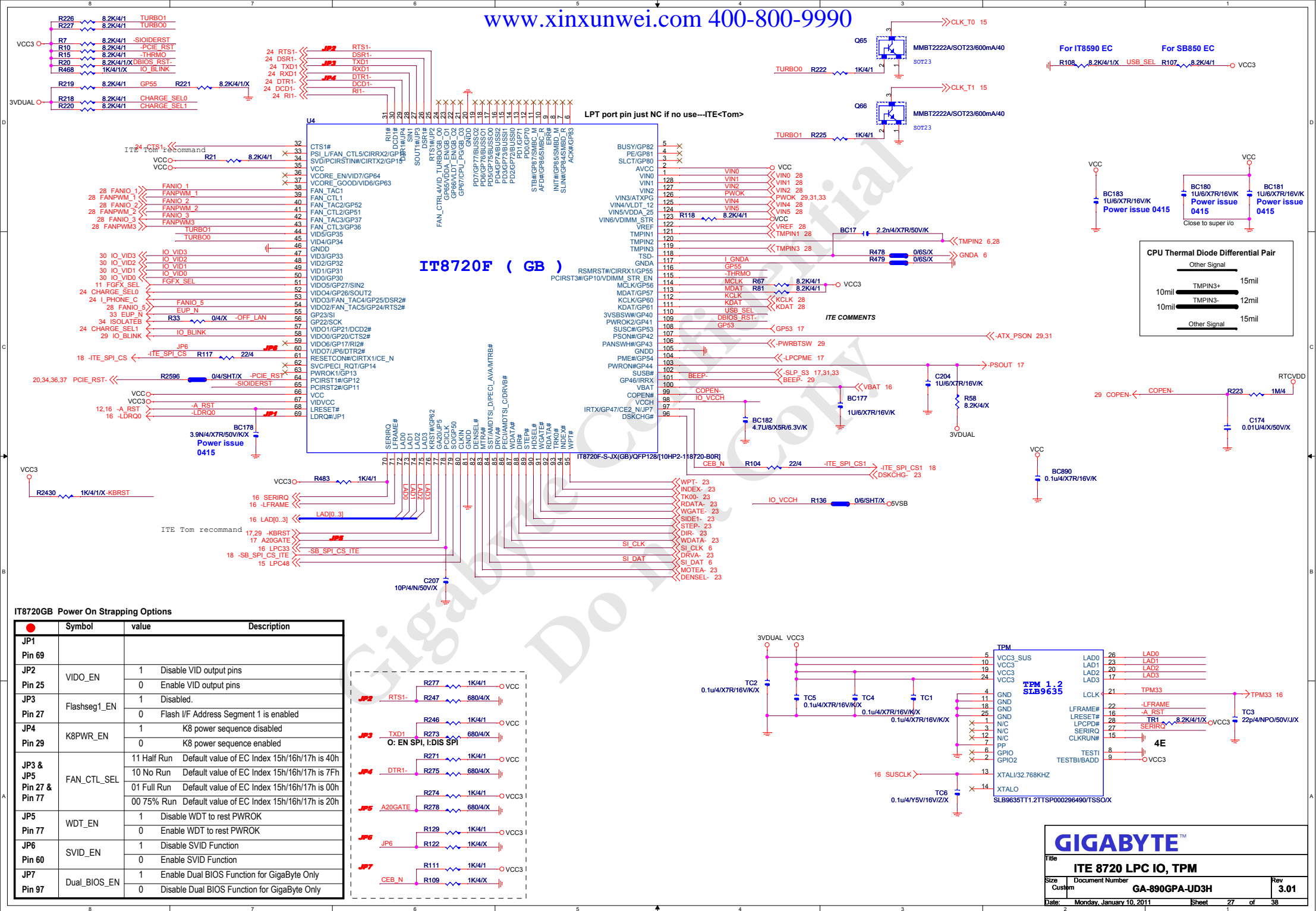


SURR BACK

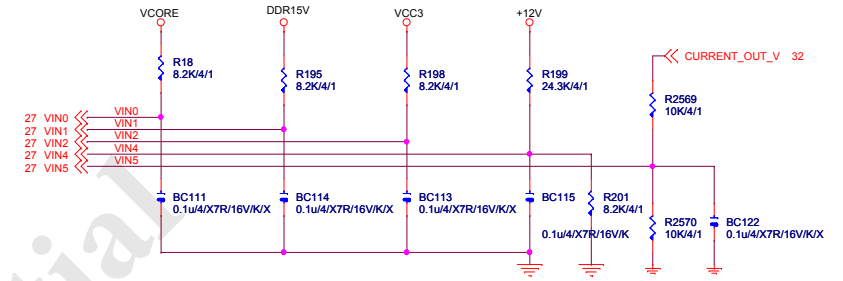
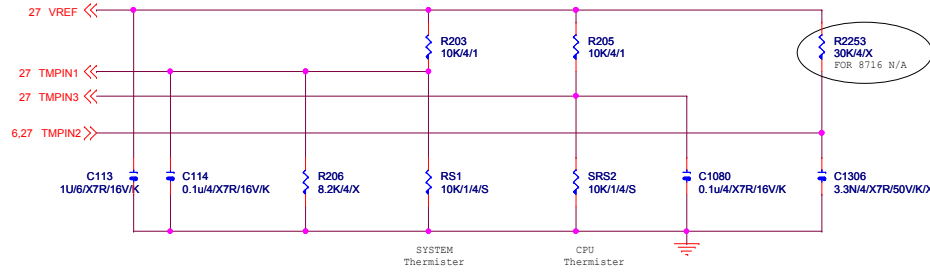


GIGABYTE

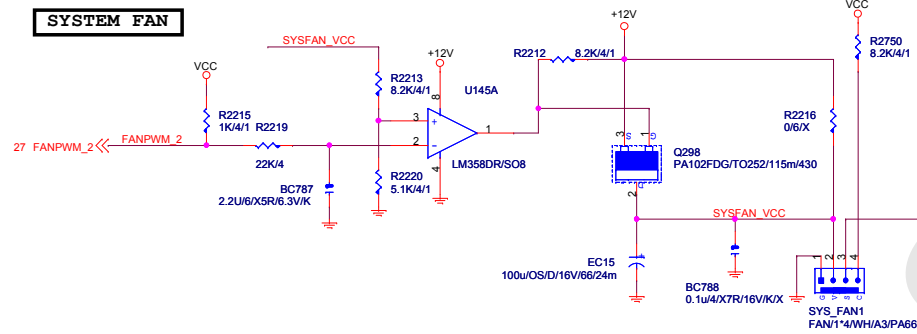
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|------------|--------------------------|----------------|
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| Size | Document Number | Rev |
| Custom | GA-890GPA-UD3H | 3.01 |
| Date: | Monday, January 10, 2011 | Sheet 26 of 38 |



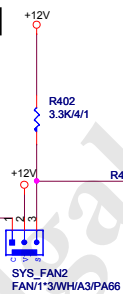
Hardware Monitor circuits



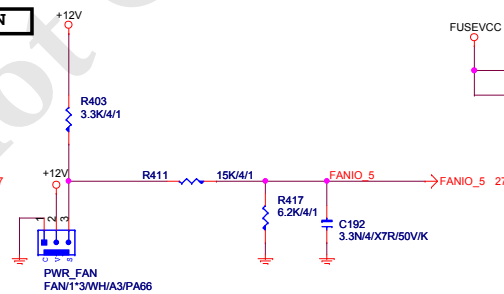
SYSTEM FAN



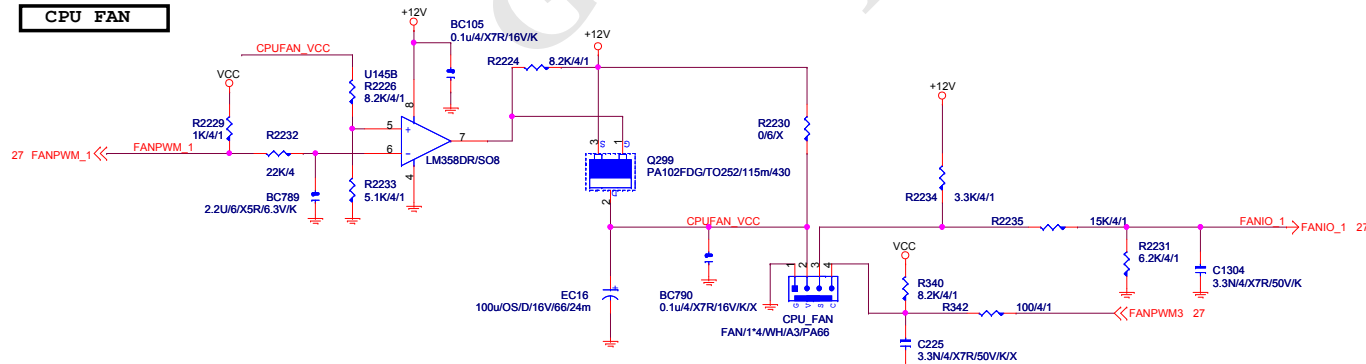
SYSTEM FAN2



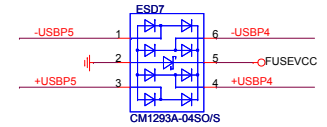
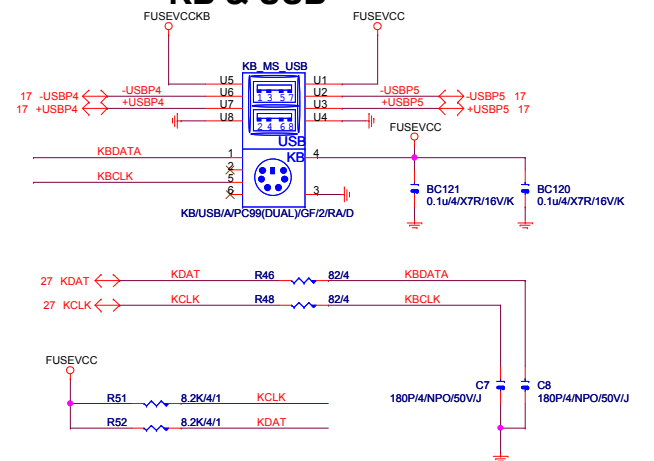
POWER FAN



CPU FAN

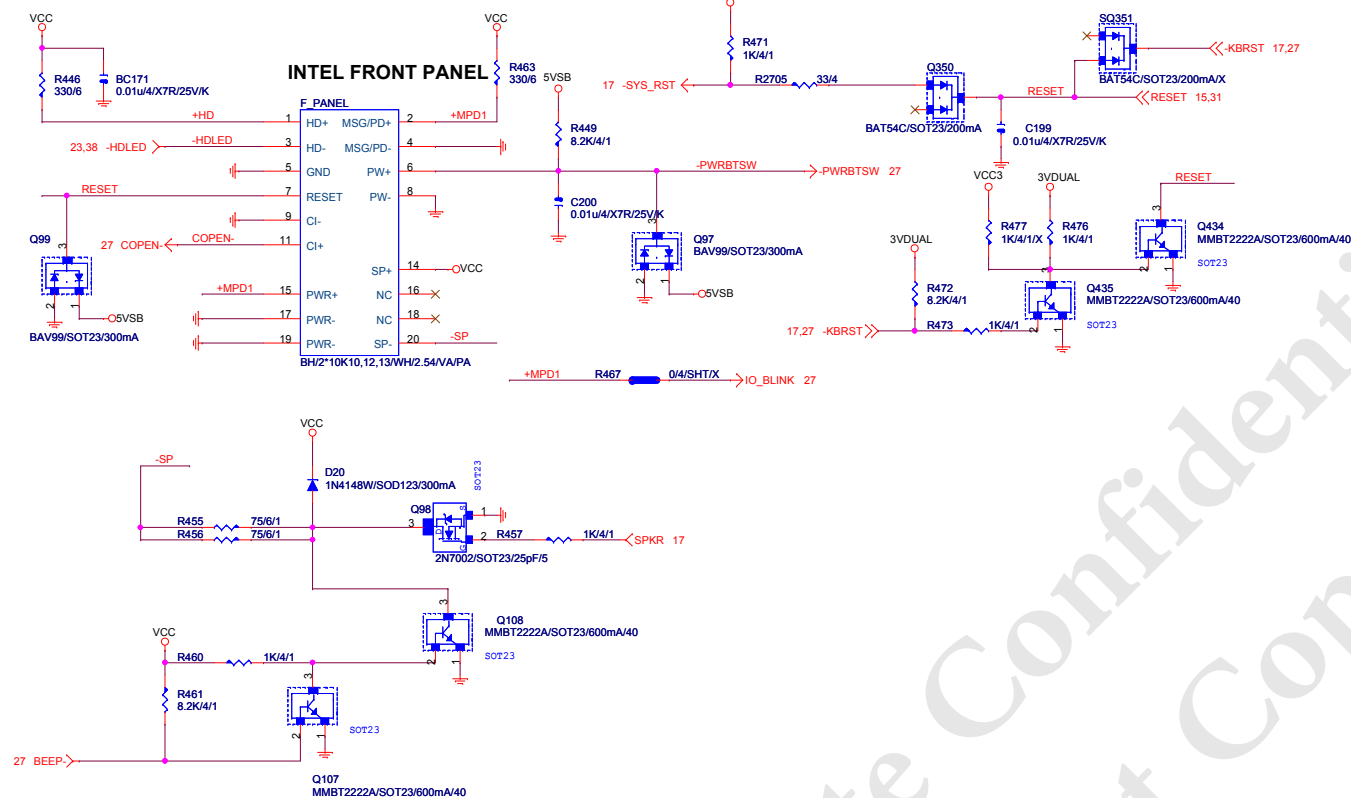


KB & USB

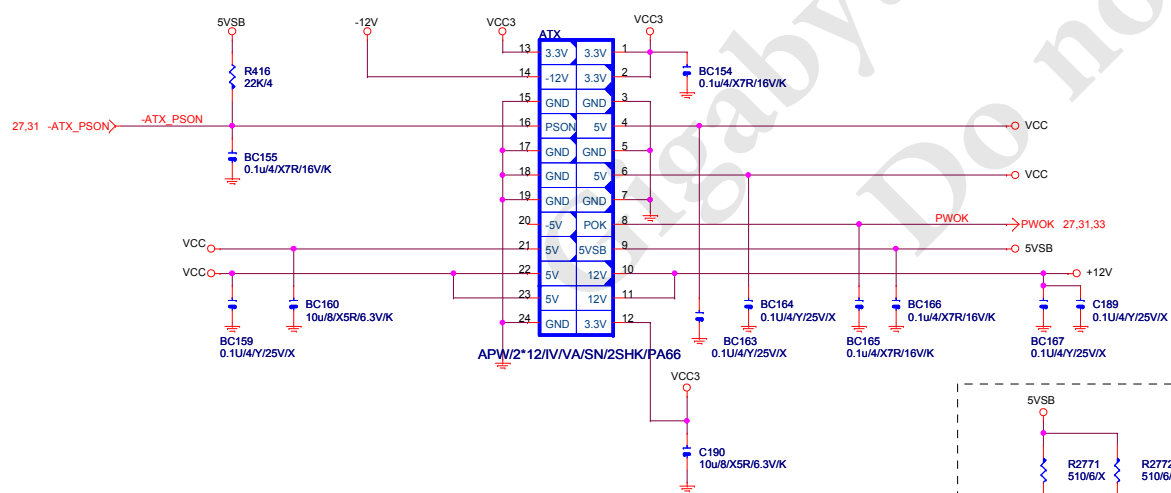


GIGABYTE™

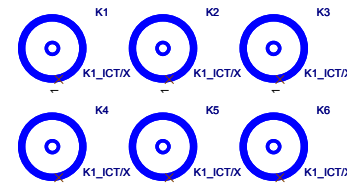
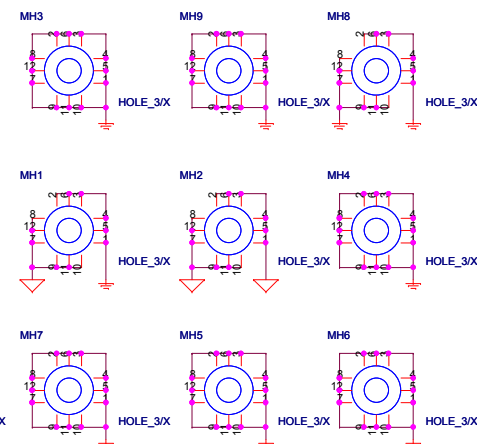
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| Title | | | FAN/HWMO KB/USB |
| Size | | | Document Number |
| Custom | | | GA-890GPA-UD3H |
| Date: | | | Monday, January 10, 2011 |
| Sheet | | | 28 of 38 |
| Rev | | | 3.01 |



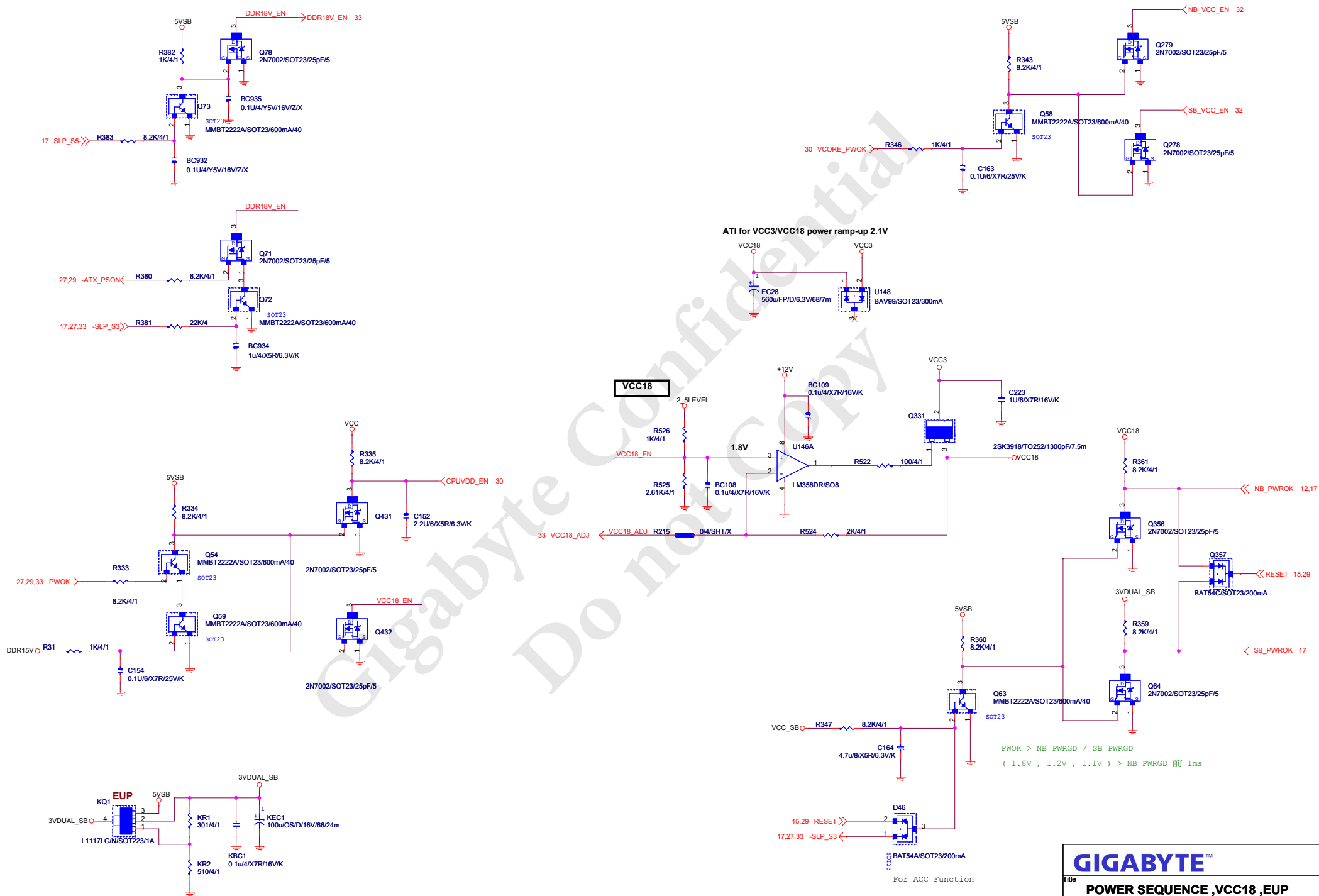
ATX POWER CONNECTOR



For Seasonic 900W
Power supply
cant Boot issue





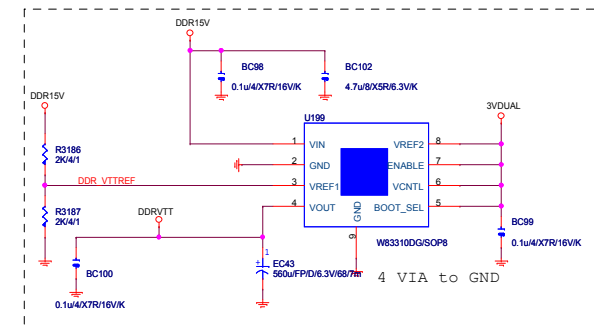
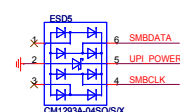
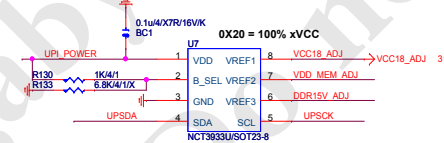
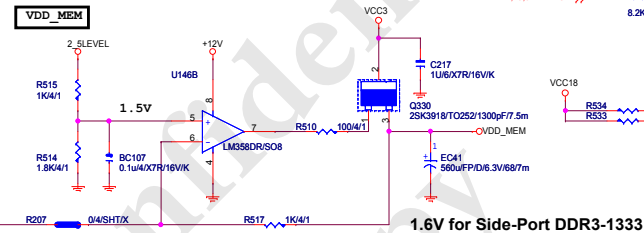
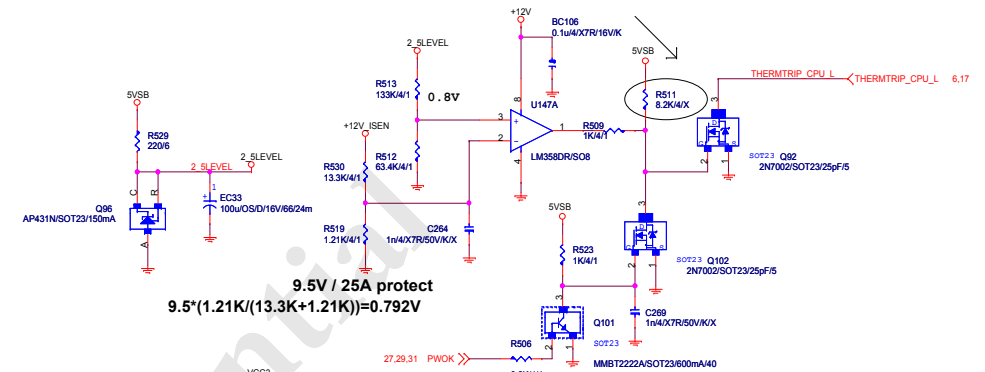


GIGABYTE

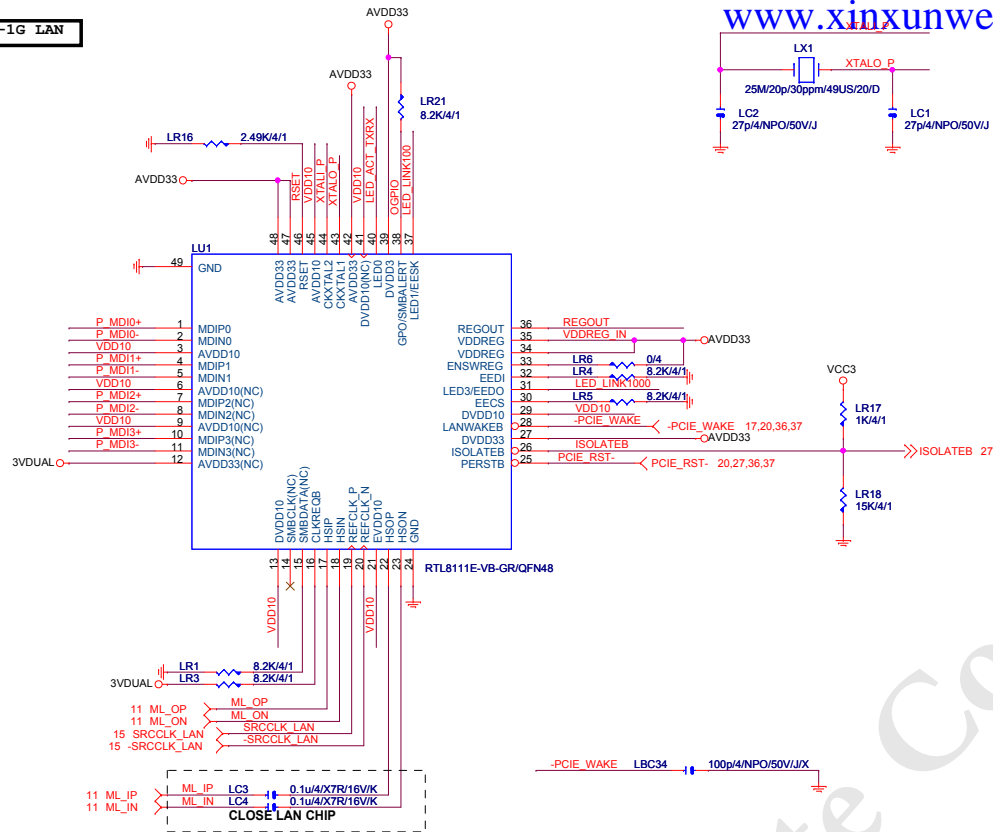
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| Title | POWER SEQUENCE ,VCC18 ,EUP |
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|--------|-----------------------|-------------|
| Size | Document Number | Rev |
| Custom | GA-890GPA-UD3H | 3.01 |

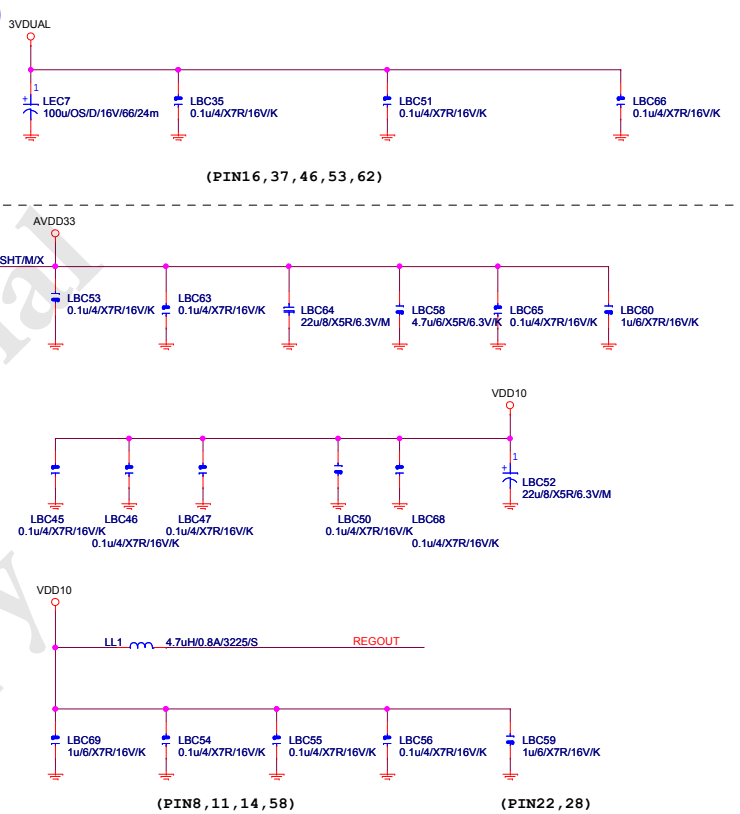
Date: Monday, January 10, 2011 Sheet 31 of 38



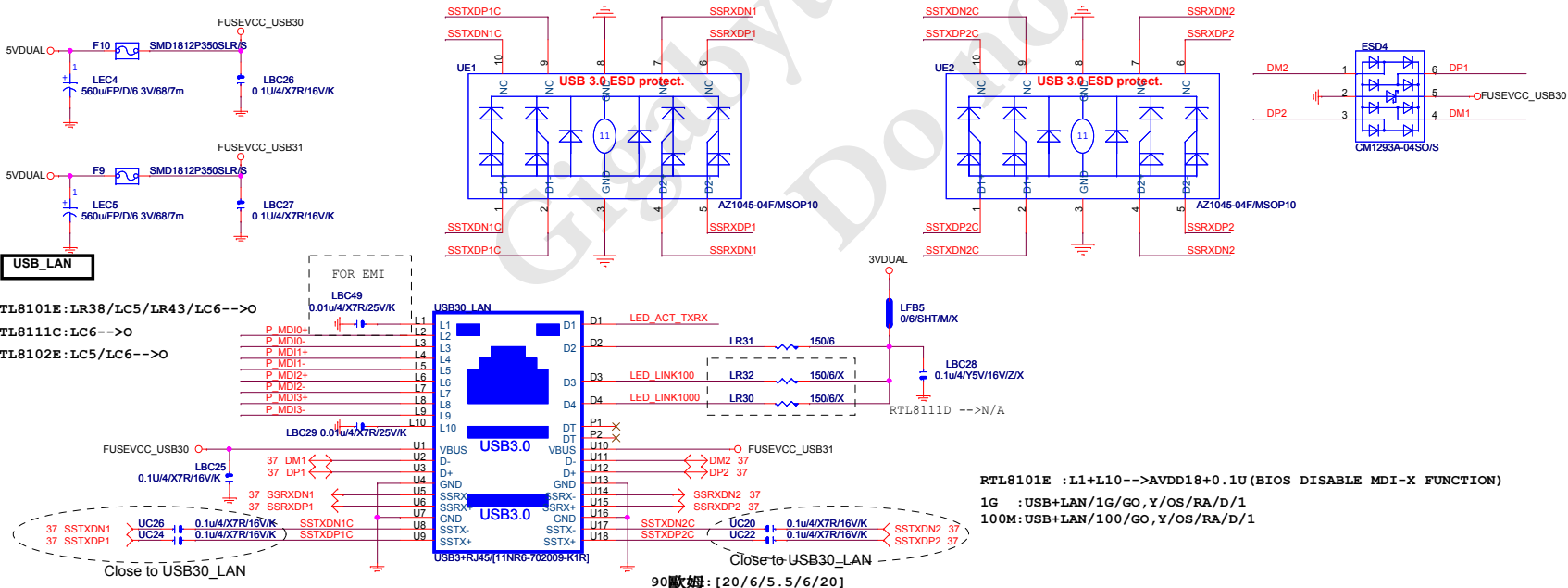
PCIE-1G LAN



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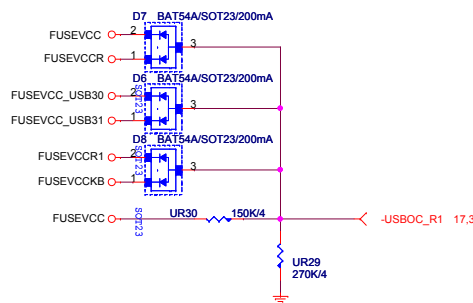
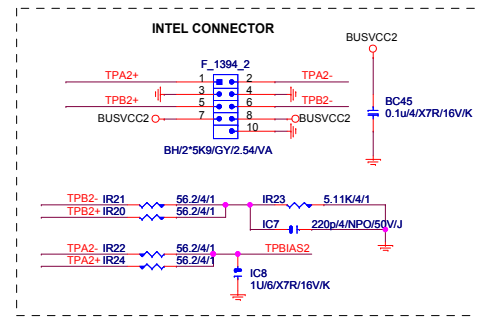
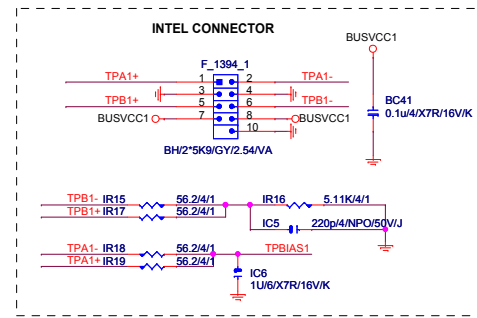
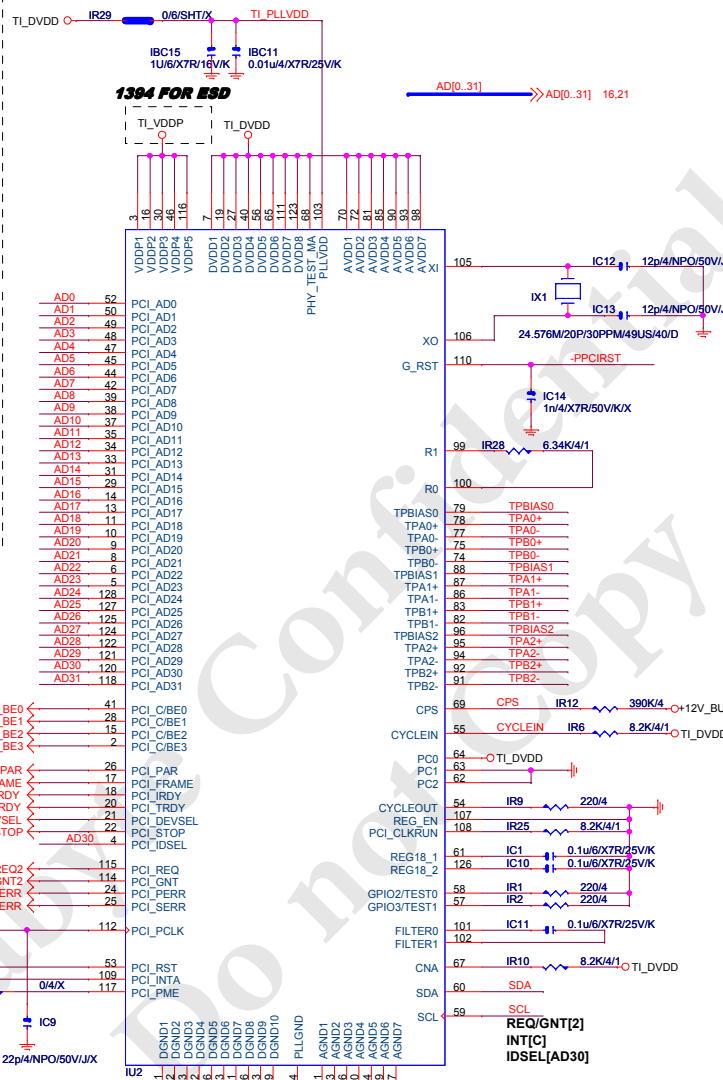
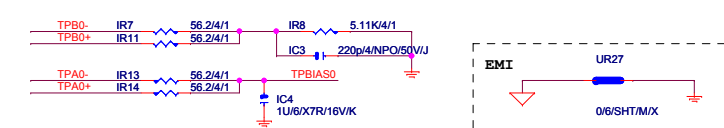
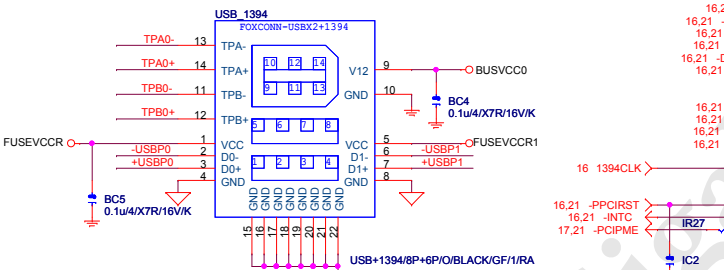
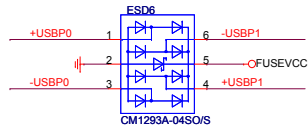
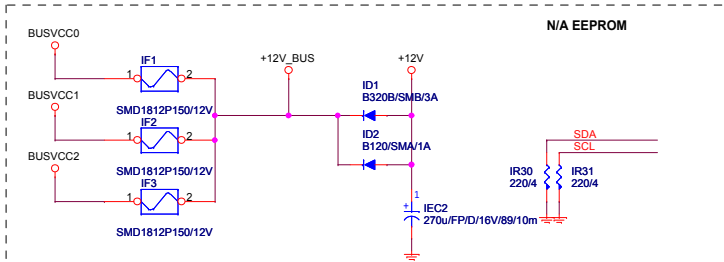
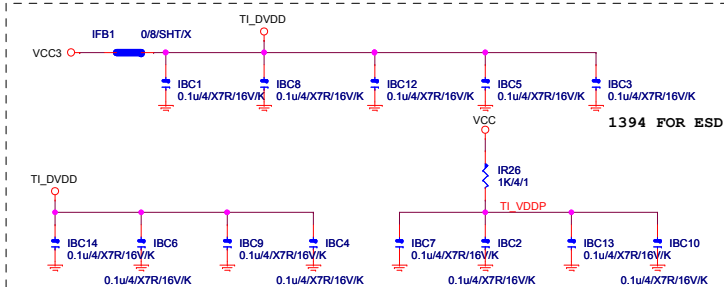
USB_LAN

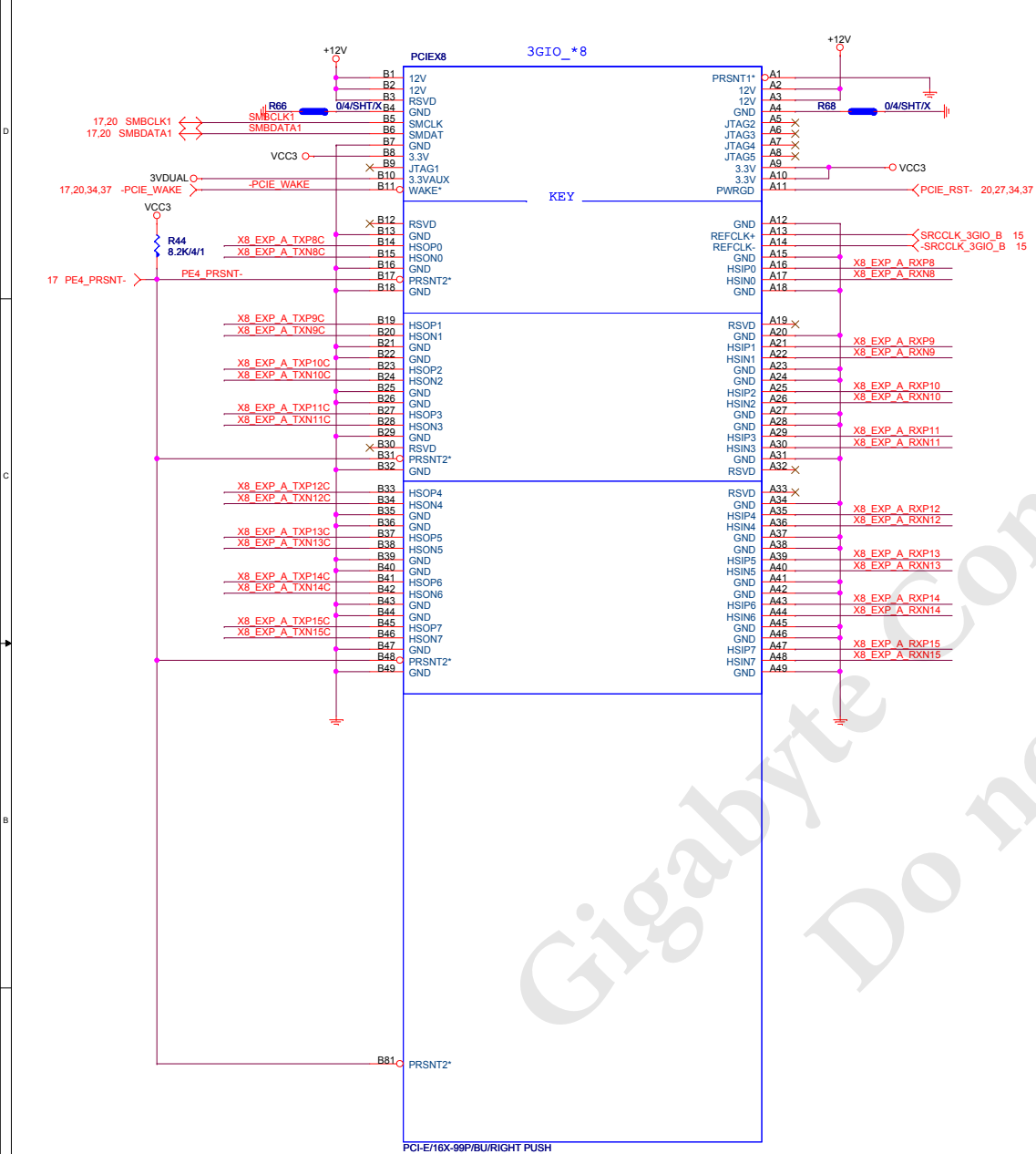


RTL8101E : L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G : USB+LAN/1G/GO, Y/OS/RA/D/1
100M: USB+LAN/100/GO, Y/OS/RA/D/1

| | | |
|-----------------------|--------------------------|----------------|
| GIGABYTE™ | | |
| Title REALTK RTL8111E | | |
| Size | Document Number | Rev |
| Custom | GA-890GPA-UD3H | 3.01 |
| Date: | Monday, January 10, 2011 | Sheet 34 of 38 |

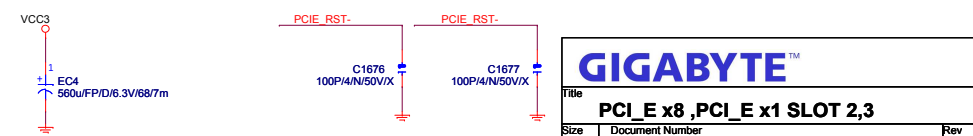
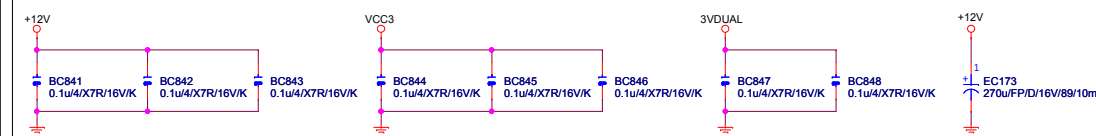
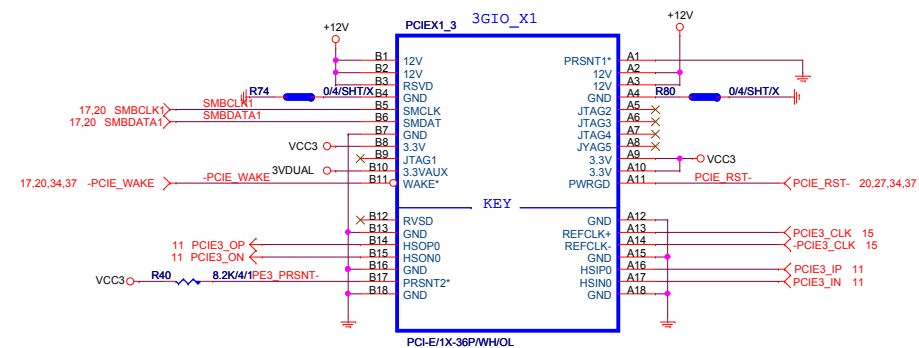
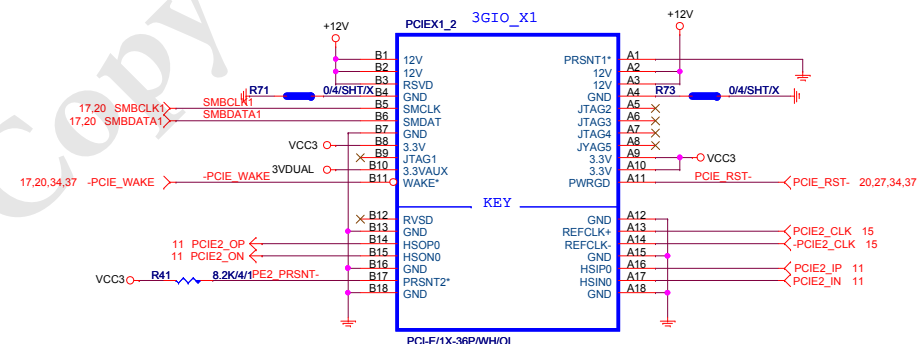
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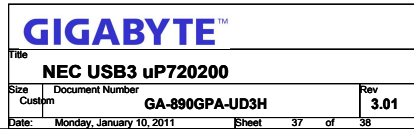




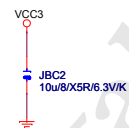
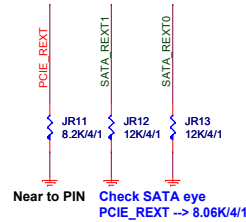
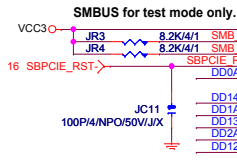
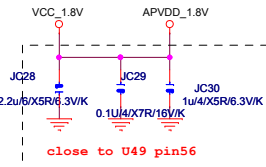
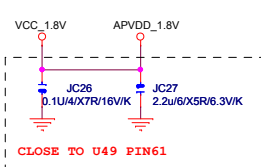
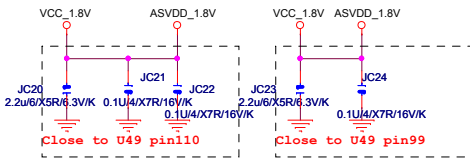
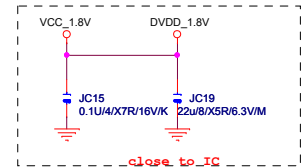
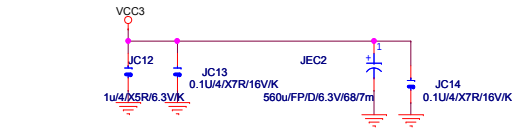
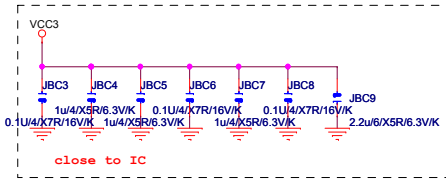
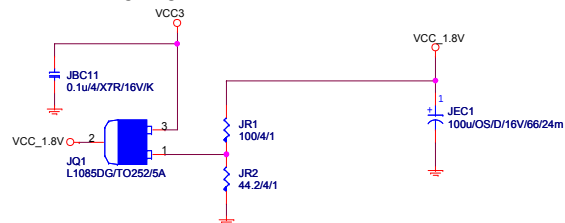
X8_EXP_A_TXP8..X8_EXP_A_TXN15C
X8_EXP_A_TXP8..X8_EXP_A_TXN15C
X8_EXP_A_RXP8..X8_EXP_A_RXN15C
X8_EXP_A_RXP8..X8_EXP_A_RXN15C

| | | | |
|----------------|-------|-----------------|-----------------|
| X8_EXP_A_TXP8 | C1683 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP8C |
| X8_EXP_A_TXN8 | C1688 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN8C |
| X8_EXP_A_TXP9 | C1685 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP9C |
| X8_EXP_A_TXN9 | C1687 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN9C |
| X8_EXP_A_TXP10 | C1682 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP10C |
| X8_EXP_A_TXN10 | C1678 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN10C |
| X8_EXP_A_TXP11 | C1684 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP11C |
| X8_EXP_A_TXN11 | C1680 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN11C |
| X8_EXP_A_TXP12 | C1681 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP12C |
| X8_EXP_A_TXN12 | C1686 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN12C |
| X8_EXP_A_TXP13 | C1679 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP13C |
| X8_EXP_A_TXN13 | C1690 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN13C |
| X8_EXP_A_TXP14 | C1693 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP14C |
| X8_EXP_A_TXN14 | C1691 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN14C |
| X8_EXP_A_TXP15 | C1689 | 0.1u4/X7R/16V/K | X8_EXP_A_TXP15C |
| X8_EXP_A_TXN15 | C1692 | 0.1u4/X7R/16V/K | X8_EXP_A_TXN15C |





3.3V to 1.8V Voltage Regulator



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